Application Note



Programming CPX-F8DE-P and the CPX-FVDA-P2 in TIA Portal V14 SP1

The application note contains an explanation how to program CPX-F8DE-P **bit oriented** and the CPX-FVDA-P2 in TIA Portal V14 SP1 V14 SP1 CPX-F8DE-P CPX-FVDA-P2

Note:

The program code is just an example. It is no must to use the program sequences 1 to 1

Title	Programming CPX-F8DE-P and the CPX-FVDA-P2 in TIA Portal V14 SP1
Version	
Document no	
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Author	
Last saved	

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1 Components/Software/Basics

Type/Name	Version Software/Firmware	IP address	Subnet mask
CPU 1516F-3 PN/DP	V 2.1	192.168.0.1	255.255.255.0
CPX-FB34 valve terminal system	REV 24	192.168.0.2	255.255.255.0
Laptop		192.168.0.100	255.255.255.0
TIA Portal V14	V14 SP1		
SIMATIC STEP7 Safety	V14 SP1		

Table 1.1:1Components/Software used

1.1 Recommended manuals / GSDML

CPX-F8DE-P manual:

https://www.festo.com/net/SupportPortal/Files/377575/CPX-F8DE-P_2015-05_8035497g1.pdf

CPX-F8DE-P short description:

https://www.festo.com/net/SupportPortal/Files/377582/CPX-F8DE-P_2015-05_8035522g1.pdf

CPX-FVDA-P2 manual:

https://www.festo.com/net/SupportPortal/Files/326376/CPX-FVDA-P2_2012-09_8022607g1.pdf

CPX GSDML:

https://www.festo.com/net/de_de/SupportPortal/default.aspx?q=CPX+GSDML&tab=4

1.2 Network Topology



1.3 CPX system

The CPX extension is following:

CPX web server	cpx / 192.168.0.2
Home Device info Diagnosis	CPX Terminal
PROFINET / I&M Ethernet	F34 E 8DI F8DI-P F8DI-P FVDO-P2 MPA 1 0 I I I I I I I I I

The valve terminal includes two CPX-F8DE-P with different M12 connection blocks. The reason is:



1.4 CPX-F8DE-P and CPX-FVDA-P2 Safety address settings

In PROFIsafe sender and receiver must have a unique identification called "F-address". At the CPX safety modules you can set the PROFIsafe address via DIL switches. Therefore you have to do following:

1. Power off the CPX system

2. Remove the 4 Screws of the connection block



3. Take out the electronic module



4. Change the DIL settings to define the F-address on the module backside



Fig. 2/2: 10-bit DIL switch for setting the PROFIsafe address - binary coded

2 Safety Application

2.1 Emergency Stop

An emergency stop contains very often two Normally Closed switches. It is used to shut off a device/machine in an emergency situation.

The circuit with a CPX-F8DE-P module on **X1-T** and the connection block **CPX-M-AB-4-M12X2-5POL-T** looks like: CPX-F8DE-P with connection block CPX-M-AB-4-M12X2-5POL-T



The recommended CPX-F8DE-P function mode is 6:

Function mode 6 – 1002 T (equivalent, with clock signal monitoring)

Signal evaluation of a two-channel switch/sensor (internal equivalent) per channel pair with individually switched power supply.

Circuit diagram	Channel pair ports					
o	то	T2	T4	T6		
	E1	E3	E5	E7		
	0 V					
	EO	E2	E4	E6		
	T1	Т3	T5	T7		

Tab. 1/21: Function mode 6 – 1002T

This function mode detects short circuits and cross-circuiting in the sensor wiring.

This function mode is especially well suited to applications that expect fast reactions (e.g. emergency stop, certified switches/sensors).

2.2 Euchner Door switch CES-AP-01-CH-SB

This safety switch is an interlocking device without guard locking. A stop command is triggered if the safety guard is opened during dangerous machine function. The safety outputs (OA and OB) can be connected to the safe inputs of a control system. Important is that the inputs must be suitable for pulsed safety signals (OSSD [Output Signal switch device] signals)

The circuit with a CPX-F8DE-P module on X1 and the connection block CPX-M-AB-4-M12X2-5POL looks like:





The recommended CPX-F8DE-P function mode is 5:

Function mode 5-1002 (equivalent)

Signal evaluation of a sensor (typically OSSD) that switches both signals of a channel pair simultaneously.

The sensor can monitor for short circuits and for cross-circuiting.

A two-channel sensor (internally equivalent) per channel pair with standard unswitched sensor power supply. T0, T2, T4, T6 run in this function mode on static 24 V DC.





2.3 Two-Hand control after EN574 type IIIC

EN574 type IIIC means that both antivalent switches have to be pressed synchronous within 500ms The circuit with a CPX-F8DE-P module on **X1-T** and the connection block **CPX-M-AB-4-M12X2-5POL-T** looks like:



The recommended CPX-F8DE-P function mode is 7:

Circuit diagram	it diagram Channel pair ports	Comments			
	Signal evaluation of 2 independent dual-chan-				
	E1 E3 E5 E7	E7	NO/ NC) per channel pair, with monitoring of		
	0 V	/		The signal change over time. At E1, E3, E5 and E7, the clock signals are	
	EO	E2	E4	E6	wired as a mirror image of E0, E2, E4, E6.
	T1	T3	T5	T7	 500 ms, a logic 1 is set in the input image of the channel pair. Before each actuation, a zero crossover is required (both normally closed contacts NC closed). Use only antivalent switches in which the one contact opens before the other contact closes. Make sure that the NO or NC switches of the sensors are connected with the matching clock signal connections of the channel pair (→ Circuit diagram). Safety evaluation only with the following connection blocks: CPX-M-AB-4-M12X2-5POL-T CPX-AB-8-KL-4POL.

2.4 Example architecture with CPX-F8DE-P





3 Programming in TIA Portal V14 SP1

3.1 Key requirements

A) You have created a new TIA Portal project with no network error:



B) You have downloaded and installed the latest CPX GSDML

danage general s	tation description	n files		
Installed GSDs	GSDs in the p	project		
Source path:	::\Users\Festo\Deskto	op GSDML-V	2.31-Festo-CPX-201	161019
Content of impo	rted path			
concent or impo				
File		Version	Language	Status

3.2 Establish a Profinet network with the CPX

A) Drag and drop the CPX entry to the network:

Safety Programming Devices & network	(S	_ - - - ×	Hardware catalog
	Topology view hetwork	view	Options
Network Connections HMI connection	🔽 🐮 🖽 🛄 🔍 ±		
		^	✓ Catalog
			<pre>dearch></pre>
PLC_1 CPU 1516F-3 PN	CPX CPX Rev 30		Filter Profile: <all></all>
	Not assigned		CPX Rev 10
			CPX Rev 30
Note			
To take the right CPX	entry (REV18, REV20 or REV30)		
Check e g via the we	pserver which Revision your node re-	ally has.	
check e.g. via the we	server which keysion your house rea	ally has.	
CC (I) C http://192.168.0.2/d	evice.htm		
🚕 📕 Highlights Festo Deutschl	퉬 Master 🕶		
CPX web server	192.168.0.2		
Home Device info Diagnosis	Device information		
PROFINET / I&M	Slot 0 - FB34-RIO		
Ethernet	PROFINET IO 2x PP R M	15	
Report	MC: 216/0 Povision: 20 S	orial number: 1E4	19101
	Slot 1 PD/PDO		A0404
	SIOT 1 - 8DI/8DO		
	Multi I/O module		
	MC: 4/0 Revision: 6 Seria	I number: DD154/	/C0
	Inputs: 8x 1 Bit		
	Outputs: 8x 1 Bit		
	Slot 2 - F8DI-P		

B) Establish the Profinet connection to the PLC :



C) Define the CPX modules from the left to the right side :

ng ▶ Ungrouped devices ▶ CPX [CPX Rev 30]					_ 🗖 🗖	×H	
		Topology view 🔒 Network	view	Devi	ice view	C	ptions
1 🔽 🖽 📰 🔍 ± 📑		Device overview					
	-	Wodule	Rack	Slot	I addr	~	Catalog
		▼ CPX	0	0		^ <	Search>
		PN-IO Interface	0	0 X1			Filter Profile:
ot	_	FB34 PNIO Module_1	0	1			Province Subsection
0	=	8DI/8DO [8DI/8DO]_1	0	2	0		
		F8DI-P bits [8DI-F]_1	0	з	16		
		F8DI-P bits [8DI-F]_2	0	4	813		
		FVDO-P2 [3DO-F]_1	0	5	1520		
		MPA1G VMPA1-FB-EMG-8 [8	-	6			Recurrentia MRA S/man
			0	-		=	Im Predmatic MPA-siprop.
			0	8			
			0	9		-	
			0	10			MPATG VMPAT-FB-EMG-8 [8D0]

As reference see the CPX webserver again. It shows you too which Profisafe DIL address is set actually:

CPX web server	192.168.0.2
Home Device info Diagnosis	Device information
PROFINET / I&M	Slot 0 - FB34-RIO
Report	PROFINET IO 2x PP RJ45
	MC: 216/0 Revision: 30 Serial number: 1F4A84C4
	Slot 1 - 8DI/8DO
	Multi I/O module
	MC: 4/0 Revision: 6 Serial number: DD154AC0
	Inputs: 8x 1 Bit
	Outputs: 8x 1 Bit
	Slot 2 - F8DI-P
	Input Module Safety
	MC: 28/1 Revision: 2 Serial number: 57014794
	F_Dest_Addr device: 1
	F_Dest_Addr configured: 0
	Functionmode for channel pair 1/0: 0
	Functionmode for channel pair 3/2: 0
	Functionmode for channel pair 5/4: 0
	Functionmode for channel pair 7/6: 0
	Slot 3 - F8DI-P
	Input Module Safety
	MC: 28/1 Revision: 2 Serial number: 57014604
	F_Dest_Addr device: 2
	F_Dest_Addr configured: 0
	Functionmode for channel pair 1/0: 0
	Functionmode for channel pair 3/2: 0
	Functionmode for channel pair 5/4: 0
	Functionmode for channel pair 7/6: 0
	Slot 4 - FVDO-P2
	Output Module Safety
	MC: 193/8 Revision: 3 Serial number: 63021301
	F_Dest_Addr device: 3
	F Dest Addr configured: 0

CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev 30] Image: CPX [CPX Rev					불 Topology view	A Network	view	🛛 🖓 Dev	ice view	
Image: constant s Texts General IO tare IO tare System constants Texts State Inputs Sili IPCFIssfe FSIL< IPC Sili	CPX [CPX Rev 30]		€ ±		Device overview					
CPX 0 0 PH40 Interface 0 0.11 PF34 Ph10 Module_1 0 1 BD1/BD0 [BD1/BD0_1] 0 2 0 PF30 Ph10 Module_1 0 3 1.6 PF30 Ph10 Interface 0 4 813 PF00 Ph10 Interface 0 5 1.520 MPA16 VMPA1 FB-EMG-8 [8 0 6 0 9 0 10 0 100 10 1 0 100 10 1 0 10 1 1 0 10 1 1 0 10 1 1 1 0 10 1 1 1 1 0 10 1 1 1 1 1 0 10 1 1 1 1 1 <td></td> <td></td> <td></td> <td>^</td> <td>Module</td> <td></td> <td> Rack</td> <td>Slot</td> <td>I addr</td> <td></td>				^	Module		Rack	Slot	I addr	
 FNHO Interface 0 0				=	CPX		0	0		1
FB34 PNIO Module_1 0 1 BDIRDO [BDIRBO]_1 0 2 0 FBDIP bits [BDIF_1] 0 3 16 FBDIP bits [BDIF_1] 0 4 813 PVDO-P2 [3DO-F_1] 0 5 1520 MPA1G VMPA1-FB.EMG-8 [8 0 6 0 0 7 0 8 0 0 10000 1 0 2 0 0 10000 1 0 5 1520 MPA1G VMPA1-FB.EMG-8 [8 0 6 0 9 0 100 1 0 10 0 9 0 100 1 1 10 10 10 0 10 1 1 10 10 10 0 10 1 1 10 10 10 10 0 10 1 1 1 10 10 10 10 10 10 1 1 1 10 10 10					PN-IO Inte	rface	0	0 X1		[
BDI/BD0 [BDI/BD0 [1] 0 2 0 FBDI/P bits [BDI/F]_1 0 3 16 FBDI/P bits [BDI/F]_2 0 4 813 FVD0-72 [3D0-F]_1 0 5 1520 MPA16 VMPA1-FB-EMG-8 [8 0 6 0 8 0 7 0 8 0 7 0 8 0 7 0 9 0 10 0 10 0 9 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 1 0 0 10 0 1 0	st				FB34 PNIO M	odule_1	0	1		
F8DI+P bits [8DI+P]_1 0 3 16 F8DI+P bits [8DI+P]_2 0 4 813 PVD0-P2 [3D0-P]_1 0 5 1520 MPA1G VMPA1-R8-EMG-8 [8 0 6 0 9 0 8 0 7 0 8 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 2 10 10 0 10 0 3 16 1 0 10 0 10 0 10 0 10 0 10 10 10 10 10 0 2 1 10 10 10 10 0 3 1 1 10 10 10 10 0 1 1 1 10 10 10 10 10 0 10 1 10 10	<u> </u>			-	8DI/8DO [8DI	/8DO]_1	0	2	0	
FBDI-P bits [8DI-F]_2 0 4 813 FVD0-P2 [3D0-F]_1 0 5 1520 MPATG VMPA1-FB-EMG-8 [8 0 6 0 8 0 7 0 8 0 9 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 10 0 10 0 0 1520 0 0 10 0 10 0 10 0 0 10 0 0 0 0 10 10 0 0 0 0 10 0 0 0 0 0 10 0 0 0 0					F8DI-P bits [8	DI-F]_1	0	3	16	
Figure 1 0 5 1520 MPA1G VMPA1-FB-EMG-8 [8 0 6 0 8 0 9 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 100* 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 0 0 10 0 0 0 10 0 0 0 10 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0<		•		-	F8DI-P bits [8	DI-F]_2	0	4	813	
MPA1G VMPA1-FB-EMG-8 [8 0 6 0 7 0 8 0 9 0 10 0 100				-	FVDO-P2 [3D0	D-F]_1	0	5	1520	
0 7 0 8 0 9 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	100				MPA1G VMPA	1-FB-EMG-8 [8	0	6		
0 8 0 9 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 10 0 1 0 1 0 1 0 1 0 1 0 1							0	7		
Image: Constant of the state of the sta							0	8		
Image: Strain of the state							0	9		
Image: Second				~			0	10		1
DI-P bits [8DI-F_1 [F8DLP : s (8DI-F]] Properties Info Diagnostics General IO tac System constants Texts General PROFIsafe PROFIsafe Inputs F_SIL: SIL3 VO addresses F_SIL: SIL3 Hardware identifier F_Block_ID: 0 F_Par_Version: 1 - F_Dest_Add: 1 -		N 1000		1000		7.642.05	^			
General IO tao System constants Texts General PROFIsafe PROFIsafe Inputs VO addresses Hardware identifier F_SIL: SIL3 Image: Sila addresses F_CRC_Length: 3-Byte-CRC F_Rar_Version: Image: Sila addresses F_Dest_Add: Image: Sila addresses	E. Martin C. Mar				<				>	
General IO tao System constants Texts General PROFIsafe	DI-P bits [8DI-F] 1 [F8DI-F	100 NIBDI-F11			Properties	Ti Info	Diagon	ostics	<u>></u>	
General PROFIsafe Inputs I/O addresses Hardware identifier F_SIL: SIL3 F_CRC_Length: 3-Byte-CRC F_Block_ID: 0 F_Par_Version: 1 F_Source_Add: 1 F_Dest_Add: 1	DI-P bits [8DI-F]_1 [F8DI-F	2 [8DI-F]]	¥_		Properties	i Info	2 Diagno	ostics	> •	
I/O addresses F_SIL: SIL3 Hardware identifier F_CRC_Length: 3-Byte-CRC F_Block_ID: 0 F_Par_Version: 1 F_Source_Add: 1	BDI-P bits [8DI-F]_1 [F8DI-F General IO tar	s [8DI-F]] System constants Texts	Y .		Properties	i Info	입 Diagno	ostics		
F_CRC_Length: 3-Byte-CRC F_Block_ID: 0 F_Par_Version: 1 F_Source_Add: 1 F_Dest_Add: 1	BDI-P bits [8DI-F]_1 [F8DI-F General 10 tag General PROFIsafe Inputs	System constants Texts PROFIsafe		<u>, 0</u>	Properties	Linfo	🖏 Diagno	ostics) 1 8	
F_Block_ID: 0 F_Par_Version: 1 F_Source_Add: 1 F_Dest_Add: 1	BDI-P bits [8DI-F]_1 [F8DI- General IO tac 9 General IPROFIsafe Inputs I/O addresses	System constants Texts PROFIsafe	F_SIL: S	, Q	Roperties	III 1160	2 Diagno	ostics		
F_Par_Version: 1 F_Source_Add: 1 F_Dest_Add: 1	General IO tac Seneral IO tac Seneral IO tac Seneral IO tac Seneral Inputs I/O addresses Hardware identifier	System constants Texts PROFIsafe F_CRC	F_SIL: S	IL3 Byte-CRC	Image: Comparison of the second sec		2 Diagno	ostics		
F_Dest_Add: 1	BDI-P bits [BDI-F]_1 [FBDI- General IO tac S General PROFIsafe Inputs I/O addresses Hardware identifier	System constants Texts PROFIsafe F_CRC	F_SIL: S _Length: 3 Block_ID: 0	IL3 Byte-CRC	C Properties		Diagno	ostics		
F_Dest_Add: 1	BDI-F bits [8DI-F]_1 [F8DI- General IO tac S General PROFIsafe Inputs I/O addresses Hardware identifier	System constants Texts PROFIsafe F_CRC F_E F_Par_	F_SIL: S Length: 3 Block_ID: 0 _Version: 1	IL3 Byte-CRC	C Properties		2 Diagno	ostics		
	BDI-P bits [BDI-F]_1 [FBDI- General IO tac 9 General PROFIsafe Inputs I/O addresses Hardware identifier	System constants Texts PROFIsafe F_CRC F_E F_Par F_Sour	F_SIL: S Length: 3 Block_ID: 0 Version: 1 rce_Add: 1	IL3 Byte-CRC	Properties		S. Diagno	ostics		
	BDI-P bits [8DI-F]_1 [F8DI-F General 10 tac 9 General PROFIsate Inputs 10 addresses Hardware identifier	System constants Texts PROFIsafe F_CRC F_E F_Par F_Sour	F_SIL: S _Length: 3 Block_ID: 0 _Version: 1 rce_Add: 1	IL3 Byte-CRC	Properties	III ▲ Info	<u>₽</u> Diagno	ostics		
	ADI-P bits [8DI-F]_1 [F8DI-F General 10 tar 4 General PROFISATE Inputs 10 addresses Hardware identifier	Signification System constants PROFIsafe F_CRC F_Par F_Sour F_D	F_SIL: S _Length: 3 Block_ID: 0 Version: 1 rce_Add: 1 est_Add: 1	IL3 Byte-CRC	Properties	₩	2 Diagno	ostics		

D) Define the PROFIsafe address parameter of each CPX safety module:

E) Define CPX IP address and Profinet name:

Safety Programming ➤ Ungro	ouped devices CPX [CPX Rev 30]			A Networ	k view		ice view
CPX [CPX Rev 30]	💌 🖽 🔣 🖽 🛄 🔍 ±		Device overview		K HOH		
		^ -	Wodule		Rack	Slot	I addr
		=	▼ CPX		0	0	
			PN-IO Inter	face	0	0 X1	
			FB34 PNIO Mo	dule_1	0	1	
C.		10	8DI/8DO [8DI/	8DO]_1	0	2	0
		•	F8DI-P bits [80	DI-F]_1	0	3	16
		2	F8DI-P bits [80	01-F]_2	0	4	813
		•	FVDO-P2 [3DC)-F]_1	0	5	1520
and the second second			MPA1G VMPA1	-FB-EMG-8 [8	0	6	
		50			0	7	
					0	8	
					0	9	
					0	10	
	100%	- 💼	<	1111	^		
PX ICPX Rev 30			O Properties	ti Info	R Diago	ostics	
General Litags Sv	stem constants Texts		Shopenes		Diagra	05005	
General							
PROFINET interice [X1]	Ethemet addresses						
General	Interface networked with						
Ethernet addresses							
Advanced options	Subnet: PN/I	IE 1					-
Hardware identifier		Add no.	weighted				1
Identification & Maintenance		Audite	v subriet				
Module parameters	ID and a set						
Hardware identifier	IP protocol						
Shared Device		et IP addre	ess in the project				
	•		iss in the project				
		IPad	dress: 192 . 168 . 0	. 2			
		Subnet	mask: 255 . 255 . 2	255.0			

Application Note – Programming CPX-F8DE-P and the CPX-FVDA-P2 in TIA Portal V14 SP1 – 1.30 $\,$

Note

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The Profinet IP address and name have to be equal in the Offline project compared to Online settings, otherwise communication problems appear. Via the Online access it is possible to change name and IP address of a device

Safety Programming 🕨 Ungro	uped devices 🕨 CPX [CPX Rev 30]
✓ Diagnostics General	Assign IP address
Diagnostic status Channel diagnostics PROFINET interface Functions Assign IP address Assign PROFINET device na Reset to factory settings	Assign IP address to the device Devices connected to an enterprise network or directly to the internet must be appropriately protected against unauthorized access, e.g. by use of firewalls and network segmentation. For more information about industrial security, please visit http://www.siemens.com/industrialsecurity
	MAC address: 00 - 00 - 00 - 00 - 00 Accessible devices IP address: 192 . 168 . 0 . 2 Subnet mask: 255 . 255 . 0

Or use the Siemens freeware Software Proneta to change name and IP address:

POP Siemens - PRONETA		
A Home		
Online Offline Comparison Configuration		
° h 🗗		
Graphical View - Online		
Щ, Щ ⊖,⊕ Т		
cde60450 cpx plc_1.profin	Set Network Parameters	
PRONETA Festo CPX-Terminal 57-1500	Please select your network parameters	
	Assign Device Name cpx	
	O IP Configuration	
	Static IP Configuration	
	IP Address	192.168. 4. 3
	Network Mask	255.255.255.0
	Use router for gateway	192.168. 4. 3

You find this Software in the Siemens Support Portal

F) Download everything to the PLC

Start safety programming 3.3

A) Insert OB82:

PLC supervisions & alarms

PROFINETIO-System (100): PN/IE_1

CPX [CPX Rev 30]

PLC alarm text lists

Local modules

Distributed I/O

La Ungrouped devices

 Documentation settings Note

🕨 📑 Common data

 \rightarrow

+ PF

Id

M

н

DB

> Additional information

Without OB82 a Safety programming mistake can create an error and the

Main program stops working. A restart of the whole system is necessary!

Data block

Add new and open



- Update

- Profile

more.

OK

Cancel



B) Open the Main safety program and insert the Global Acknowledgment function block:

Note

 \rightarrow

1. If you take as safety input for the HW signal then in error case it freezes and works not anymore! Use e.g. a normal input of a DI module. In this case the signal 0 of CPX-8DE is taken (address %10.0).

	Device overview					2.4
-	Module	 Rack	Slot	l address	Q address	Туре
	✓ CPX	0	0			CPX Rev 30
	PN-IO Interface	0	0 X1			CPX
	FB34 PNIO Module_1	0	1			FB34 PNIO Module
	8DI/8DO [8DI/8DO]_1	0	2	0	0	8DI/8DO [8DI/8DO]

Note

2. If you use the instruction ACK_GL, you do not have to provide a user acknowledgment for each F-I/O of the F-runtime group via the ACK_REI tag of the F-I/O DB.

C) Insert the Bit commands for CPX-F8DE-P modes at F-module 1 and 2:

Background info:

If you are using the CPX GSDML bit entry then you can't use the Move command function.

evice overview							
Module	 Rack	Slot	I address	Q address	Туре		✓ Catalog
▼ CPX	0	0			CPX Rev 30	- ^	<search></search>
PN-IO Interface	0	0 X1			CPX		Filter Profile:
FB34 PNIO Module_1	0	1			FB34 PNIO Module		
8DI/8DO [8DI/8DO]_1	0	2	0	0	8DI/8DO [8DI/8DO]	🗏	
F8DI-P bits [8DI-F]_1	0	3	16	17	F8DI-P bits [8DI-F]		
F8DI-P bits [8DI-F]_2	0	4	813	814	F8DI-P bits [8DI-F]		Analog modules
FVDO-P2 [3DO-F]_1	0	5	1520	1520	FVDO-P2 [3DO-F]	1	CPX-P modules
MPA1G VMPA1-FB-EMG-8 [8	0	6		21	MPA1G VMPA1-FB		CPX-safety module
	0	7					F8DI-P bits (8D
	0	8					F8DI-P word [8L

In such case it is a must to set the mode bit by bit!

Safety Pro	gramming PLC_1	CPU 1516F-3 F	N/DP] ▶ Program t	olocks ▶ Ma	in_Safety_R1	G1 [FB1]	
<u></u>		_ .	KX	All Con 4%	C-1 X	(0.000	la la
юя юя 🖻		9 3 3 1	a - 🗆 🖬 🍖 🖗	9 (m Vii 😵	• = '≡ '≡	1 CI	0, 2	8
Main_S	arety_RIGI	Data tuna	Default value	Potain	Accorcible f	Write	Vicible in	Setnoint
	Mode V1 T Rit0	Bool	false	Non-retain	Accessible I	vvrita		Serboint
	Mode X1_T_Bit1	Bool	false	Non-retain				
11	Mode_X1_T_Bit2	Bool	falce	Non-retain				
2 📶 🔳	Mode X1 T Bit3	Bool	false	Non-retain				
3 -00 =	Mode X1 T Bit4	Bool	false	Non-retain				
4 📶 =	Mode_X1_T_Bit5	Bool	false	Non-retain				
5 🤕 🗉	Mode_X1_T_Bit6	Bool	false	Non-retain				
6 📶 =	Mode_X1_T_Bit7	Bool	false	Non-retain				
#Mode #Mode	e_X1_T_Bit0	_	Network CH0 CP2 (Emerge	c 2 for d X-F8DE ency Sto	lefinitio - P modu op - Mod	n of Ile 1 e 6		
#Mode	%Q3.2 *Tag_4 = 	_						
#Mode	%Q3.3 "Tag_5 =_X1_T_Bit3 —	_						





Note

1. As reference for the function mode see chapter 2 $% \left({{{\mathbf{x}}_{i}}} \right)$

2. The Output variable depends on the HW config.

Device overview					
1 Module	Rac	k Slot	I address	Q address	Туре
▼ CPX	0	0			CPX Rev 30
PN-IO Interface	0	0 X1			CPX
FB34 PNIO Module_1	0	1			FB34 PNIO Module
8DI/8DO [8DI/8DO]_1	0	2	0	0	8DI/8DO [8DI/8DO
F8DI-P bits [8DI-F]_1	0	3	16	17	F8DI-P bits [8DI-F]
F8DI-P bits [8DI-F]_2	0	4	813	814	F8DI-P bits [8DI-F]
FVDO-P2 [3DO-F]_1	0	5	1520	1520	FVDO-P2 [3DO-F]
MPA1G VMPA1-FB-EMG-8 [8	0	6		21	MPA1G VMPA1-FB-



Note

For the function mode the start byte (QB3 and QB10) are important. It includes CH1/0 of the CPX-F8DE-P $\ensuremath{\mathsf{F8DE-P}}$

Bit samp	les for t	the output	data					
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	1/0	1/0
	Operati	ng mode: 1 0	= channel-l = module-l	based passi based passi	ivation vation			
	1 = Ack	nowledgme	nt of a chan	nel error				
1	в	4	2	1	8	4	2	1
CH3/2	Function	n mode for a	hannel pair	7/6	Function	n mode for a	hannel pair	5/4
2	8	4	2	1	8	4	2	1
CH1/0	Function	n mode for a	hannel pair	3/2	Function	n mode for o	hannel pair	1/0

Tab. 1/7: Bit pattern for output data (F usage data, bytes 0, 1 and 2)



Note 3. The mode and Bit relation you find in following table

Value	Binary
Zero	0000
One	0001
Two	0010
Three	0011
Four	0100
Five	0101
Six	0110
Seven	0111
Eight	1000
Nine	1001
Ten	1010
Eleven	1011
Twelve	1100
Fhirteen	1101
Fourteen	1110
Fivteen	1111

D) Download everything and check the behaviour of the safety input variables via watch table:

Project tree		Safet	y Programming	PLC_1 [CPU 1516	5F-3 PN/DP] 🕨 Wa	tch and force tab	les 🔸 Watch tal	ole_1
Devices								
		*	? 🟥 🕼 🕼 1	1 % 2 00 00				
		i	Name	Address	Display format	Monitor value	Modify value	9
 Safety Programming 	0	1		%11.0	Bool	TRUE		
💕 Add new device		2		%11.4	Bool	TRUE		
🛔 Devices & networks		3		%11.1	Bool	FALSE		63
PLC_1 [CPU 1516F-3 PN/DP]	V 🔒	4		%11.5	Bool	FALSE		
Device configuration		5		%18.0	Bool	TRUE		
😵 Online & diagnostics		6		%18.4	Bool	TRUE		
Safety Administration	0	7		Add new>				
🕨 🔂 Program blocks	•							
🕨 🙀 Technology objects								
External source files								
🕨 🌄 PLC tags	•							
PLC data types	•							
🔻 詞 Watch and force tables								
📑 Add new watch table								
Force table								
Watch table 1								



Note

1. The reasons for the safety input addresses are

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	E7	E5	E3	E1	E6	E4	E2	EO
	Input im	lage			_	2		
1	Q7	Q5	Q3	Q1	Q6	Q4	Q2	QO
	Qualific Qx = 1: Qx = 0:	ation bits Signal Ex is Signal Ex is channel er	s valid s invalid, in ror/module	correct input	t function in	accordance	with functi	on mode,

Tab. 1/8: Bit pattern of input data (F-usage data, byte 0 and byte 1)



Note

2. In the webserver you can check the assigned mode too!

Outputs. ON T DIC
Slot 2 - F8DI-P
Input Module Safety
MC: 28/1 Revision: 2 Serial number: 57014794
F Dest Addr device: 1
Functionmode for channel pair 1/0: 6
Functionmode for channel pair 3/2: 7
Functionmode for channel pair 5/4: 0
Functionmode for channel pair 7/6: 0
Slot 3 - F8DI-P
Input Module Safety
MC: 28/1 Revision: 2 Serial number: 57014604
F_Dest_Addr device: 2
Functionmode for channel pair 1/0: 5
Functionmode for channel pair 3/2: 0
Functionmode for channel pair 5/4: 0
Functionmode for channel pair 7/6: 0

E) Write a small sample project to energize CH0 in network 5 of the CPX-FVDA-P2:



Note 1. The internal circuit of the CPX-FVDA-P2 is looking like this:



Note

2. If you activate the BitO then you power on CHO too and the supply in CPX backplane for the valves is forwarded safety

Bit patt Byte	ern of the o	butput d Bit 6	ata: byte Bit 5	0 and byte 1 Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Byte 0	Reserved	Test pu activate	lse ed	Reserved		Nomina	l status		
		CH2	CH1			CH2	CH1	СНО	
	0	0 = acti 1 = dea	vate ctivate	0		0 = off 1 = on			
Byte 1	Channel- wise passiva- tion	Reserve	ed	Data direction	Reserv ed	Acknow CH2	Acknowledgment CH2 CH1 CH0		
0	0 = off 1 = On	0		0 = Device to host (fixed value)	0	 Change Low → High = acknowledgment or Permanent 1 = auto-a ledgment 		ligh = user t or uto-acknow	

Tab. 1/7: Bit pattern of the output data (F-user data, byte 0 and byte 1)

D) Download everything and press the 2-Hand control:



After pressing the 2-Hand Control the safety logic is active and the valves have no error anymore:



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Application Note – Programming CPX-F8DE-P and the CPX-FVDA-P2 in TIA Portal V14 SP1– 1.30

4 Further function mode examples

4.1 SICK Light curtain type "deTec 4 Core"

The deTec4 Core safety light curtain is an electro-sensitive protective device (ESPE) consisting of a sender and receiver.

A series of parallel infrared light beams form a protective field between sender and receiver that protects the hazardous area (hazardous point, access, and hazardous area protection). When one or more beams are completely interrupted, the safety light curtain reports the interruption in the light path to the secure output signal switching devices (OSSDs) by a signal change. The machine or its control must evaluate the signals reliably (e.g., by means of a safety controller or a safety relay) and bring an end to the dangerous state.

Sender and receiver automatically synchronize themselves optically. An electrical connection between both components is not required.



Figure 1: Sender and receiver

The Sender and receiver have following pin allocation:

System connection (M12, 5-pin)



Figure 27: System connection (M12, 5-pin)

Pin	Wire color	Sender	Receiver
1	Brown	+24 V DC (power supply input)	+24 V DC (power supply input)
2	White	Reserved	OSSD1 (output signal switching device 1)
3	Blue	0 V DC (power supply input)	0 V DC (power supply input)
4	Black	Reserved	OSSD2 (output signal switching device 2)
5	Gray	Not yet assigned	Not yet assigned

Table 2: System connection pin assignment (M12, 5-pin)

Via the Festo NEDU connector you can combine the Sender and Receiver:

1.3 Sensors

1.3.1 Plug	connectors							
Part no.	Order code	Name	Picture	Quantity	Price	Total	Case layer	ID
2839867	NEDU-L2R1- V10-M12G5- M12G5	Push-in T connector		1	15,15 EUR	15,15 EUR	1	5



In this case the right function mode could be 5:

Circuit diagram	ns	Chan	nel pai	r ports	-	Comments
А , ц. ц.	0	T0/ 24 V	T2/ 24 V	T4/ 24 V	T6/ 24 V	Signal evaluation of a sensor (typically OSSD), which switches both signals of the channel
	0	E1	E3	E5	E7	pair simultaneously. Short-circuit and cross-circuit monitoring can
	0	0 V		8		take place through the sensor.
		EO	E2	E4	E6	Example A
*	0	T1/ FE	T3/ FE	T5/ FE	T7/ FE	A dual-channel switch/sensor (internally equivalent) per channel pair with uniformly unclocked sensor supply.
B	0	24 V	24V	24V	24V	In this function mode, T0, T2, T4 and T6 are at
		E1	E3	E5	E7	- Static 24 V DC.
		0 V	4		4	Example B OSSD sensor
		EO	E2	E4	E6	USSU sensor
	0	T1	T3	T5	T7	1
	0	FE co senso conne modu	nnectio or via th ector fit ile	n of the M12 ting of	e plug the	

Function mode 5 - 1002 (equivalent)

The connection block have to be the cage clamp variant or

onnection block	Pin allocation X1, X2	Pin allocation X3, X4
0 40 40 40 10 10 50 40 40 40 10 10 50 40 40 40 10 10 50 40 40 40 0 10 10 50 40 40 40 0 10 10 50 40 40 0 0 10 10 50 40 40 40 0 0 10 10 50 40 40 40 0 0 10 10 50 40 40 40 40 0 10 10 50 40 40 40 40 0 10 10 50 40 40 40 0 10 10 50 40 40 40 0 10 10 50 40 40 40 0 0 0 0 0 0 0 0 0 0 0 0 0	$\begin{array}{c} 3 \\ 0 \\ 2 \\ 2 \\ 1 \\ 2 \\ 1 \\ 4 \\ \end{array} \begin{array}{c} 3 \\ 0 \\ 0 \\ 0 \\ 1 \\ 2 \\ 1 \\ 1 \\ 2 \\ 1 \\ 1 \\ 1 \\ 2 \\ 1 \\ 1$	$\begin{array}{c} 3 \\ 3 \\ 2 \\ 2 \\ 3 \\ 4 \end{array} \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_4 \\ x_5 \\ x_6 \\ x_6$

Keine Indexeinträge gefunden.