S7-200 Quick Reference Information

To help you find information more easily, this section summarizes the following information:

- Special Memory Bits
- Descriptions of Interrupt Events
- Summary of S7-200 CPU Memory Ranges and Features
- High-Speed Counters HSC0, HSC1, HSC2, HSC3, HSC4, HSC5
- S7-200 Instructions

Table G-1 Special Memory Bits

Special Memory Bits			
SM0.0	Always On	SM1.0	Result of operation = 0
SM0.1	First Scan	SM1.1	Overflow or illegal value
SM0.2	Retentive data lost	SM1.2	Negative result
SM0.3	Power up	SM1.3	Division by 0
SM0.4	30 s off / 30 s on	SM1.4	Table full
SM0.5	0.5 s off / 0.5 s on	SM1.5	Table empty
SM0.6	Off 1 scan / on 1 scan	SM1.6	BCD to binary conversion error
SM0.7	Switch in RUN position	SM1.7	ASCII to hex conversion error

Table G-2 Interrupt Events in Priority Order

Event Number	Interrupt Description	Priority Group	Priority in Group
8	Port 0: Receive character	Communications (highest)	0
9	Port 0: Transmit complete		0
23	Port 0: Receive message complete		0
24	Port 1: Receive message complete		1
25	Port 1: Receive character		1
26	Port 1: Transmit complete		1
19	PTO 0 complete interrupt	Discrete (middle)	0
20	PTO 1 complete interrupt		1
0	I0.0, Rising edge		2
2	I0.1, Rising edge		3
4	I0.2, Rising edge		4
6	I0.3, Rising edge		5
1	I0.0, Falling edge		6
3	I0.1, Falling edge		7
5	I0.2, Falling edge		8
7	I0.3, Falling edge		9
12	HSC0 CV=PV (current value = preset value)		10
27	HSC0 direction changed		11
28	HSC0 external reset		12
13	HSC1 CV=PV (current value = preset value)		13
14	HSC1 direction input changed		14
15	HSC1 external reset		15
16	HSC2 CV=PV		16
17	HSC2 direction changed		17
18	HSC2 external reset		18
32	HSC3 CV=PV (current value = preset value)		19
29	HSC4 CV=PV (current value = preset value)		20
30	HSC4 direction changed		21
31	HSC4 external reset		22
33	HSC5 CV=PV (current value = preset value)		23
10	Timed interrupt 0	Timed (lowest)	0
11	Timed interrupt 1		1
21	Timer T32 CT=PT interrupt		2
22	Timer T96 CT=PT interrupt		3

Table G-3 Memory Ranges and Features for the S7-200 CPUs

Description		CPU 221	CPU 222	CPU 224	CPU 224XP CPU 224XPsi	CPU 226
User program size with run mode edit without run mode edit		 4096 bytes 4096 bytes	 4096 bytes 4096 bytes	 8192 bytes 12288 bytes	 12288 bytes 16384 bytes	 16384 bytes 24576 bytes
User data size		2048 bytes	2048 bytes	8192 bytes	10240 bytes	10240 bytes
Process-image input register		I0.0 to I15.7	I0.0 to I15.7	I0.0 to I15.7	I0.0 to I15.7	I0.0 to I15.7
Process-image output register		Q0.0 to Q15.7	Q0.0 to Q15.7	Q0.0 to Q15.7	Q0.0 to Q15.7	Q0.0 to Q15.7
Analog inputs (read only)		AIW0 to AIW30	AIW0 to AIW30	AIW0 to AIW62	AIW0 to AIW62	AIW0 to AIW62
Analog outputs (write only)		AQW0 to AQW30	AQW0 to AQW30	AQW0 to AQW62	AQW0 to AQW62	AQW0 to AQW62
Variable memory (V)		VB0 to VB2047	VB0 to VB2047	VB0 to VB8191	VB0 to VB10239	VB0 to VB10239
Local memory (L)[1]		LB0 to LB63	LB0 to LB63	LB0 to LB63	LB0 to LB63	LB0 to LB63
Bit memory (M)		M0.0 to M31.7	M0.0 to M31.7	M0.0 to M31.7	M0.0 to M31.7	M0.0 to M31.7
Special Memory (SM) Read only		SM0.0 to SM179.7 SM0.0 to SM29.7	SM0.0 to SM299.7 SM0.0 to SM29.7	SM0.0 to SM549.7 SM0.0 to SM29.7	SM0.0 to SM549.7 SM0.0 to SM29.7	SM0.0 to SM549.7 SM0.0 to SM29.7
Timers		256 (T0 to T255)	256 (T0 to T255)	256 (T0 to T255)	256 (T0 to T255)	256 (T0 to T255)
Retentive on-delay	1 ms	T0, T64	T0, T64	T0, T64	T0, T64	T0, T64
	10 ms	T1 to T4, and T65 to T68	T1 to T4, and T65 to T68	T1 to T4, and T65 to T68	T1 to T4, and T65 to T68	T1 to T4, and T65 to T68
	100 ms	T5 to T31, and T69 to T95	T5 to T31, and T69 to T95	T5 to T31, and T69 to T95	T5 to T31, and T69 to T95	T5 to T31, and T69 to T95
On/Off delay	1 ms	T32, T96	T32, T96	T32, T96	T32, T96	T32, T96
	10 ms	T33 to T36, and T97 to T100	T33 to T36, and T97 to T100	T33 to T36, and T97 to T100	T33 to T36, and T97 to T100	T33 to T36, and T97 to T100
	100 ms	T37 to T63, and T101 to T255	T37 to T63, and T101 to T255	T37 to T63, and T101 to T255	T37 to T63, and T101 to T255	T37 to T63, and T101 to T255
Counters		C0 to C255	C0 to C255	C0 to C255	C0 to C255	C0 to C255
High-speed counters		HC0 to HC5	HC0 to HC5	HC0 to HC5	HC0 to HC5	HC0 to HC5
Sequential control relays (S)		S0.0 to S31.7	S0.0 to S31.7	S0.0 to S31.7	S0.0 to S31.7	S0.0 to S31.7
Accumulator registers		AC0 to AC3	AC0 to AC3	AC0 to AC3	AC0 to AC3	AC0 to AC3
Jumps/Labels		0 to 255	0 to 255	0 to 255	0 to 255	0 to 255
Call/Subroutine		0 to 63	0 to 63	0 to 63	0 to 63	0 to 127
Interrupt routines		0 to 127	0 to 127	0 to 127	0 to 127	0 to 127
Positive/negative transitions		256	256	256	256	256
PID loops		0 to 7	0 to 7	0 to 7	0 to 7	0 to 7
Ports		Port 0	Port 0	Port 0	Port 0, Port 1	Port 0, Port 1

[1] LB60 to LB63 are reserved by STEP 7-Micro/WIN, version 3.0 or later.

Table G-4 High-Speed Counters HSC0, HSC3, HSC4, and HSC5

Mode	HSC0			HSC3	HSC4			HSC5
	Clk	Direction	Reset	Clk	Clk	Direction	Reset	Clk
0	I0.0			I0.1	I0.3			I0.4
1	I0.0		I0.2		I0.3		I0.5	
2								
3	I0.0	I0.1			I0.3	I0.4		
4	I0.0	I0.1	I0.2		I0.3	I0.4	I0.5	
5								
Mode	**HSC0**				**HSC4**			
	Clk Up	**Clk Down**	**Reset**		**Clk Up**	**Clk Down**	**Reset**	
6	I0.0	I0.1			I0.3	I0.4		
7	I0.0	I0.1	I0.2		I0.3	I0.4	I0.5	
8								
Mode	**HSC0**				**HSC4**			
	Phase A	**Phase B**	**Reset**		**Phase A**	**Phase B**	**Reset**	
9	I0.0	I0.1			I0.3	I0.4		
10	I0.0	I0.1	I0.2		I0.3	I0.4	I0.5	
11								
Mode	**HSC0**			**HSC3**				
	Clk			**Clk**				
12	Q0.0			Q0.1				

Table G-5 High-Speed Counters HSC1 and HSC2

Mode	HSC1				HSC2			
	Clk	Clk Down	Reset	Start	Clk	Direction	Reset	Start
0	I0.6				I1.2			
1	I0.6		I1.0		I1.2		I1.4	
2	I0.6		I1.0	I1.1	I1.2		I1.4	I1.5
3	I0.6	I0.7			I1.2	I1.3		
4	I0.6	I0.7	I1.0		I1.2	I1.3	I1.4	
5	I0.6	I0.7	I1.0	I1.1	I1.2	I1.3	I1.4	I1.5
Mode	**HSC1**				**HSC2**			
	Clk Up	**Clk Down**	**Reset**	**Start**	**Clk Up**	**Clk Down**	**Reset**	**Start**
6	I0.6	I0.7	I1.0		I1.2	I1.3		
7	I0.6	I0.7	I1.0		I1.2	I1.3	I1.4	
8	I0.6	I0.7	I1.0	I1.1	I1.2	I1.3	I1.4	I1.5
Mode	**Phase A**	**Phase B**	**Reset**	**Start**	**Phase A**	**Phase B**	**Reset**	**Start**
9	I0.6	I0.7			I1.2	I1.3		
10	I0.6	I0.7	I1.0		I1.2	I1.3	I1.4	
11	I0.6	I0.7	I1.0	I1.1	I1.2	I1.3	I1.4	I1.5

Boolean Instructions

LD	Bit	Load
LDI	Bit	Load Immediate
LDN	Bit	Load Not
LDNI	Bit	Load Not Immediate
A	Bit	AND
AI	Bit	AND Immediate
AN	Bit	AND Not
ANI	Bit	AND Not Immediate
O	Bit	OR
OI	Bit	OR Immediate
ON	Bit	OR Not
ONI	Bit	OR Not Immediate
LDBx	IN1, IN2	Load result of Byte Compare IN1 (x:<, <=,=, >=, >, <>I) IN2
ABx	IN1, IN2	AND result of Byte Compare IN1 (x:<, <=,=, >=, >, <>) IN2
OBx	IN1, IN2	OR result of Byte Compare IN1 (x:<, <=,=, >=, >, <>) IN2
LDWx	IN1, IN2	Load result of Word Compare IN1 (x:<, <=,=, >=, >, <>) IN2
AWx	IN1, IN2	AND result of Word Compare IN1 (x:<, <=,=, >=, >, <>)I N2
OWx	IN1, IN2	OR result of Word Compare IN1 (x:<, <=,=, >=, >, <>) IN2
LDDx	IN1, IN2	Load result of DWord Compare IN1 (x:<, <=,=, >=, >, <>) IN2
ADx	IN1, IN2	AND result of DWord Compare IN1 (x:<, <=,=, >=, >, <>)IN2
ODx	IN1, IN2	OR result of DWord Compare IN1 (x:<, <=,=, >=, >, <>) IN2
LDRx	IN1, IN2	Load result of Real Compare IN1 (x:<, <=,=, >=, >, <>) IN2
ARx	IN1, IN2	AND result of Real Compare IN1 (x:<, <=,=, >=, >, <>) IN2
ORx	IN1, IN2	OR result of Real Compare IN1 (x:<, <=,=, >=, >, <>) IN2
NOT		Stack Negation
EU		Detection of Rising Edge
ED		Detection of Falling Edge
=	Bit	Assign Value
=I	Bit	Assign Value Immediate
S	Bit, N	Set bit Range
R	Bit, N	Reset bit Range
SI	Bit, N	Set bit Range Immediate
RI	Bit, N	Reset bit Range Immediate
LDSx	IN1, IN2	Load result of String Compare IN1 (x: =, <>) IN2
ASx	IN1, IN2	AND result of String Compare IN1 (x: =, <>) IN2
OSx	IN1, IN2	OR result of String Compare IN1 (x: =, <>) IN2
ALD		And Load
OLD		Or Load
LPS		Logic Push (stack control)
LRD		Logic Read (stack control)
LPP		Logic Pop (stack control)
LDS	N	Load Stack (control)
AENO		And ENO

Math, Increment, and Decrement instructions

+I +D +R	IN1, OUT IN1, OUT IN1, OUT	Add Integer, Double Integer or Real IN1+OUT=OUT
-I -D -R	IN1, OUT IN1, OUT IN1, OUT	Subtract Integer, Double Integer, or Real OUT-IN1=OUT
MUL	IN1, OUT	Multiply Integer (16*16->32)
*I *D *R	IN1, OUT IN1, OUT IN1, IN2	Multiply Integer, Double Integer, or Real IN1 * OUT = OUT
DIV	IN1, OUT	Divide Integer (16/16->32)
/I /D, /R	IN1, OUT IN1, OUT IN1, OUT	Divide Integer, Double Integer, or Real OUT / IN1 = OUT
SQRT	IN, OUT	Square Root
LN	IN, OUT	Natural Logarithm
EXP	IN, OUT	Natural Exponential
SIN	IN, OUT	Sine
COS	IN, OUT	Cosine
TAN	IN, OUT	Tangent
INCB INCW INCD	OUT OUT OUT	Increment Byte, Word or DWord
DECB DECW DECD	OUT OUT OUT	Decrement Byte, Word, or DWord
PID	TBL, LOOP	PID Loop

Timer and Counter Instructions

TON	Txxx, PT	On-Delay Timer
TOF	Txxx, PT	Off-Delay Timer
TONR	Txxx, PT	Retentive On-Delay Timer
BITIM	OUT	Beginning Interval Timer
CITIM	IN, OUT	Calculate Interval Timer
CTU	Cxxx, PV	Count Up
CTD	Cxxx, PV	Count Down
CTUD	Cxxx, PV	Count Up/Down

Real Time Clock Instructions

TODR	T	Read Time of Day clock
TODW	T	Write Time of Day clock
TODRX	T	Read Real Time Clock Extended
TODWX	T	Set Real Time Clock Extended

Program Control Instructions

END		Conditional End of Program
STOP		Transition to STOP Mode
WDR		WatchDog Reset (300 ms)
JMP	N	Jump to defined Label
LBL	N	Define a Label to Jump to
CALL	N [N1,...]	Call a Subroutine [N1, ... up to 16 optional parameters]
CRET		Conditional Return from SBR
FOR NEXT	INDX,INIT,FINAL	For/Next Loop
LSCR SCRT CSCRE SCRE	N N	Load, Transition, Conditional End, and End Sequence Control Relay
DLED	IN	Diagnostic LED

Move, Shift, and Rotate Instructions		
MOVB MOVW MOVD MOVR	IN, OUT IN, OUT IN, OUT IN, OUT	Move Byte, Word, DWord, Real
BIR BIW	IN, OUT IN, OUT	Move Byte Immediate Read Move Byte Immediate Write
BMB BMW BMD	IN, OUT, N IN, OUT, N IN, OUT, N	Block Move Byte, Word, DWord
SWAP	IN	Swap Bytes
SHRB	DATA, S_BIT, N	Shift Register Bit
SRB SRW SRD	OUT, N OUT, N OUT, N	Shift Right Byte, Word, DWord
SLB SLW SLD	OUT, N OUT, N OUT, N	Shift Left Byte, Word, DWord
RRB RRW RRD	OUT, N OUT, N OUT, N	Rotate Right Byte, Word, DWord
RLB RLW RLD	OUT, N OUT, N OUT, N	Rotate Left Byte, Word, DWord
Logical Instructions		
ANDB ANDW ANDD	IN1, OUT IN1, OUT IN1, OUT	Logical AND of Byte, Word, and DWord
ORB ORW ORD	IN1, OUT IN1, OUT IN1, OUT	Logical OR of Byte, Word, and DWord
XORB XORW XORD	IN1, OUT IN1, OUT IN1, OUT	Logical XOR of Byte, Word, and DWord
INVB INVW INVD	OUT OUT OUT	Invert Byte, Word and DWord (1's complement)
String Instructions		
SLEN	IN, OUT	String Length
SCAT	IN, OUT	Concatenate String
SCPY	IN, OUT	Copy String
SSCPY	IN, INDX, N, OUT	Copy Substring from String
CFND	IN1, IN2, OUT	Find First Character within String
SFND	IN1, IN2, OUT	Find String within String

Table, Find, and Conversion Instructions		
ATT	DATA, TBL	Add data to table
LIFO FIFO	TBL, DATA TBL, DATA	Get data from table
FND= FND<> FND< FND>	TBL, PTN, INDX TBL, PTN, INDX TBL, PTN, INDX TBL, PTN, INDX	Find data value in table that matches comparison
FILL	IN, OUT, N	Fill memory space with pattern
BCDI IBCD	OUT OUT	Convert BCD to Integer Convert Integer to BCD
BTI ITB ITD DTI	IN, OUT IN, OUT IN, OUT IN, OUT	Convert Byte to Integer Convert Integer to Byte Convert Integer to Double Integer Convert Double Integer to Integer
DTR TRUNC ROUND	IN, OUT IN, OUT IN, OUT	Convert DWord to Real Convert Real to Double Integer Convert Real to Double Integer
ATH HTA ITA DTA RTA	IN, OUT, LEN IN, OUT, LEN IN, OUT, FMT IN, OUT, FM IN, OUT, FM	Convert ASCII to Hex Convert Hex to ASCII Convert Integer to ASCII Convert Double Integer to ASCII Convert Real to ASCII
DECO ENCO	IN, OUT IN, OUT	Decode Encode
SEG	IN, OUT	Generate 7-segment pattern
ITS DTS RTS	IN, FMT, OUT IN, FMT, OUT IN, FMT, OUT	Convert Integer to String Convert Double Integer to String Convert Real to String
STI STD STR	STR, INDX, OUT STR, INDX, OUT STR, INDX, OUT	Convert Substring to Integer Convert Substring to Double Integer Convert Substring to Real
Interrupt Instructions		
CRETI		Conditional Return from Interrupt
ENI DISI		Enable Interrupts Disable Interrupts
ATCH DTCH	INT, EVNT EVNT	Attach Interrupt routine to event Detach event
Communications Instructions		
XMT RCV	TBL, PORT TBL, PORT	Freeport transmission Freeport receive message
NETR NETW	TBL, PORT TBL, PORT	Network Read Network Write
GPA SPA	ADDR, PORT ADDR, PORT	Get Port Address Set Port Address
High-Speed Instructions		
HDEF	HSC, MODE	Define High-Speed Counter mode
HSC	N	Activate High-Speed Counter
PLS	Q	Pulse Output