TRS Star CompactFlash Card
Industrial-Grade Datasheet

Revision 1.4
06/2006

TRS* Tele-Radio-Space GmbH
Industriestrasse 5
D-76297 Stutensee
Germany
Fax +49(0)910387
Email: info@trs-space.de
www.trs-space.de
www.trs-star.com

Revision History

Revision 1.0 Initial release

Revision 1.1 Change on page 6, section 1.1 General Description, MTBF from >3,000,000 to >2 500 000 hours
Change on page 11, section 2.3 System Performance, table 2.3 Performance, Maximum Performance, Sequential Write from 9MB/sec to 8MB/sec
Change on page 11, section 2.4 System Reliability, table 2.4 Reliability, Endurance, standard temperature from 1 800 000 to 2 000 000
Add on page 13, section 2.6 Capacity Specifications, table 2.6 Model Capacities, the new options and the new model with 16GBit Flash chip
Change on page 85 and 86, section 6 CIS (Card Information Structure) Description, table 6 Card Information Structure, the Info String2, Article-No and the Ordering-No to the newest Version
Change on page 87, section 7 Ordering Information Industrial Grade, table 7 Ordering Information from old to the newest Version
Change on page 88, section 8 TRS* Star Back-Side Label Specification, the picture from the Back-Side Label
Change on page 88, section 8 TRS* Star Back-Side Label Specification, table 8. Barcode Information
Update on page 92, section 12 EU Declaration of Conformity the Product Family

Revision 1.2 Change on page 10, section 2.2 Power Requirements,
Table 2.2 Power Requirements.
Change on page 14, section 3.1 CF Card Pin Assignments and Pin Type, table 3.1 the input pin type 3 in input pin type 2.
Change on page 19, section 3.3.2 Input Characteristics, Type 1, Input Voltage 5.0V from 2.4V to 2.6V, Type 2, Input Voltage 5.0V from2.0V to 2.4V, delete Type 3.

Revision 1.3 Change on page 19, section 3.3.2 Input Characteristics, Type 1, Input Voltage from 3.3V and 5.0V to 3,3V ±10% and 5.0V ±10%.
Remove on page 87, section 7 Ordering Information Industrial-Grade a mistake at the Pos. “f”
Change on page 88, section 8 TRS* Star Back-Side Label Specification, the picture from the Back-Side Label
Change on page 88, section 8 TRS* Star Back-Side Label Specification, table 8. Barcode Information to Back-Side Label Specification

Revision 1.4 Add on page 4, section Instructions.
Change on page 13, section 2.4 System Reliability, Table 2.4 Reliability, Endurance extended temperature from 800 000 to 2 000 000.
Add on page 89, section 7 Ordering Information Industrial-Grade, Controller, Options for realtime application.
Add on page 90, section 8 TRS* Star Back-Side Label Specification, table 8. WEEE EAR registry no.

Change on page 109, section 14. UL Technical Report to section 14. NRTL (UL) Technical Report

Instructions

The information contained in this technical document is subject to change without previous notice.

TRS* takes no responsibility for (no guarantees) the unit to be marketable or suitable for a particular purpose.

Furthermore, TRS* will not be held liable for errors in this technical documentation as well as coincidental or sequential damages in connection with the delivery, performance and use of this material.

The device listed in this technical documentation was designed and manufactured for use in OA equipment.

In case of using the device for applications such as control and safety equipment for transportation(aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment(trunk lines), nuclear power control equipment and medical or other equipment for life support.

TRS* assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in these specification sheets.

TRS* Tele-Radio-Space GmbH
Industriestraße5
D-76297 Stutensee

Table of Contents

1. General Description

The TRS* Tele-Radio-Space GmbH called TRS Star CompactFlash® Memory Card (CF) provide high capacity solid-state flash memory. The CompactFlash cards support True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot, and with a Type II PCMCIA adapter can be used in any system that has a PCMCIA Type II or Type III socket.

All Standard Grade ATA Flash Storage products use Flash memory chips from original Suppliers.
In addition to the mass storage specific Flash memory chips, the Standard ATA products include an on-card intelligent controller from Hyperstone that provides a high level interface to the host computer. This interface allows a host computer to issue commands to the memory card to read or write blocks of memory. The host addresses the card in 512 byte sectors. Each sector is protected by a powerful Error Correcting Code (ECC, 4 bit). The Standard ATA product's on-card intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. Once the Industrial ATA product has been configured by the host, it appears to the host as a standard ATA (IDE) disk drive. Additional ATA commands have been provided to enhance system performance.

Figure 1 is a system block diagram; see Section 2 for detailed specifications.

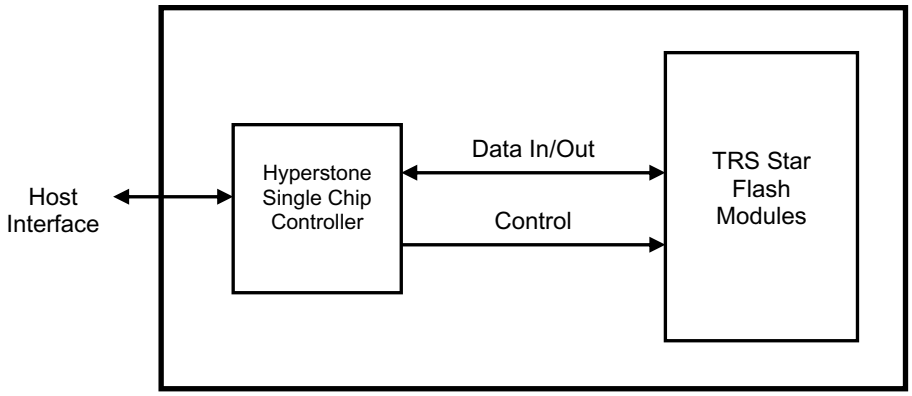


Figure 1. System Block Diagram

1.1 General Description

The Industrial-Grade ATA products provide the following system features:

- Up to 8 GB of mass storage data for CompactFlash
- PC Card ATA protocole compatible, True IDE Mode compatible
- Very low CMOS power, Very high performance
- Very rugged, Low weight, Noiseless, Low Profile
- +5.0 Volts or +3.3 Volts operation
- Automatic error correction and retry capabilities
- Supports power down commands and sleep modes
- Non-volatile storage (no battery required)
- MTBF >2 500 000 hours, Minimum 10 000 insertions
- Standard and Extended Temperature

1.2 CompactFlash Specification

CompactFlash Memory Cards are fully compatible with the CompactFlash Specification Rev. 2.0 and will be compatible with Revision 2.1 published by the CompactFlash Association. Contact the CompactFlash Association for more information:

CompactFlash Association
P.O. Box 51537
Palo Alto, CA 94303
USA
Phone: 415-843-1220
FAX: 415-493-1871
www.compactflash.org

1.3 PCMCIA Standard

CompactFlash Memory Cards are fully electrically compatible with the following PCMCIA - specifications:

- *PCMCIA PC Card Standard*, 7.0, February 1999
- *PCMCIA PC Card ATA Specification*, 7.0, February 1999

These specifications may be obtained from:

PCMCIA
2635 North First St., Ste. 209
San Jose, CA 95131
USA
Phone: 408-433-2273
FAX: 408-433-9558

1.4. ATA Specification

CompactFlash Memory Cards are fully compatible with the ATA Specification published by ANSI:

American National Standard X3.221: AT Attachment Interface for Disk Drives

This document can be ordered from Global Engineering Documents by calling 1-800-854-7179.

1.5. Functional Description

Industrial ATA products contain a high level, intelligent subsystem as shown in Figure 1-1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of memory cards. These capabilities include the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Host independence from details of erasing and programming flash memory.
- Sophisticated system for managing defects
  (analogous to systems found in magnetic disk drives).
- Sophisticated system for error recovery including a powerful error correction code (ECC).
- Power management for low power operation.

1.5.1. Technology Independence

The 512-byte sector size of the Industrial ATA product is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the card. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Since the card uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support the Industrial ATA products today will be able to access future TRS* Tele-Radio-Space GmbH cards built with NAND Flash Technology without having to update or change host software.

1.5.2. Defect and Error Management

Industrial-Grade TRS* Star CompactFlash Cards contain a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary the cards will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space.
The soft error rate for Industrial-Grade TRS* Star CompactFlash Cards is much lower than the magnetic disk drive specification. In the extremely rare case a read error does occur, the card has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid-state construction, give the TRS* Star CompactFlash Cards unparalleled reliability.

1.5.3. Wear Levelling

Wear Levelling is an intrinsic part of the operation of TRS* Tele-Radio-Space GmbH CompactFlash Cards using NAND memory. The CF WEAR LEVEL command is supported as a NOP operation to maintain backward compatibility with existing software utilities.

1.5.4. Using the Erase Sector and Write without Erase Commands

TRS* Tele-Radio-Space GmbH Industrial-Grade TRS* Star CompactFlash Cards support the ERASE SECTOR and WRITE WITHOUT ERASE commands. In some applications, write operations may be faster if the addresses being written are first erased with the ERASE SECTORS command. WRITE WITHOUT ERASE behaves as a normal write command and no performance gain results from its use.

1.5.5. Automatic Sleep Mode

A unique feature of the TRS* Star Industrial-Grade CompactFlash cards is automatic entrance and exit from sleep mode. Upon completion of a command, the card will enter sleep mode to conserve power if no further commands are received within 5 msec. The host does not have to take any action for this to occur. In most systems, the card is in sleep mode except when the host is accessing it, thus conserving power. Note that the delay from command completion to entering sleep mode can be adjusted. When the host is ready to access the card and it is in sleep mode, any command issued to the card will cause it to exit sleep and respond. The host does not have to follow the ATA protocol of issuing a reset first. It may do this if desired, but it is not needed. By not issuing the reset, performance

is improved through the reduction of overhead but this must be done only for the TRS* Star CompactFlash Cards as other ATA products may not support this feature.

1.5.6. Power Supply Requirements

This is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ± 10% or 5.00 volts ± 10%. Per the PCMCIA specification Section 2.1.1, the host system must apply 0 volts in order to change a voltage range. This same procedure of providing 0 volts to the card is required if the host system applies an input voltage outside the desired voltage by more than 15%. This means less than 4.25 volts for the 5.00 volt range and less than 2.75 volts for the 3.30 volt range.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1 System Enviromental Specifications

Table 2.1 Enviromental Specifications

		Standard Temp. Range	Extended Temp. Rang
Temperature	Operating Non-Operating	0°C to +65°C -20°C to +85°C	-40°C to +80°C -50°C to +100°C
Humidty	Operating & Non-Operating	5% to 95%, non-condensing	5% to 95%, non-condensing
Acoustic Noise	Operating & Non-Operating	0dB	0dB
Vibration	Operating & Non-Operating	*30 G peak-to-peak maximum*	*30 G peak-to-peak maximum*
Shock	Operating & Non-Operating	3 000 G maximum	3 000 G maximum
Altitude (relative to sea level)	Operating & Non-Operating	80 000 feet maximum	80 000 feet maximum

2.2 System Power Requirements

Table 2.2 Power Requirements

		Standard Temp. Range		Extended Temp. Rang	
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		**3.3V ±10%**	**5V ± 10%**	**3.3V ±10%**	**5V ±10%**
Maximum Average Value See Notes below	up to 512MB Sleep	120 µA	250 µA	120 µA	250 µA
	over 512 MB Sleep	240 µA	500 µA	240 µA	500 µA
	Reading	30 mA RMS	38 mA RMS	30 mA RMS	38 mA RMS
	Writing	35 mA RMS	45 mA RMS	35 mA RMS	45 mA RMS
	Read/Write Peak	40 mA	50 mA	40 mA	50 mA

NOTES: All values quoted are typical at 25° C and nominal supply voltage.
Sleep mode currently is specified under the condition that all card inputs are static CMOS levels and in a “Not Busy” operating state.

2.3 System Performance

All performance timings assume the card controller is in the default (i.e., fastest) mode.

Table 2.3 Performance

Controller Overhead	Command to DRQ -Sleep to write -Sleep to read Reset to ready	 2.5 msec maximum 20 msec maximum 50 msec typical 400 msec maximum
Data Transfer Rate To/From Flash		20.0 MB/sec burst
Data Transfer Rate To/From Host		16.0 MB/sec burst
Maximum Performance	Sequential Read	10 MB/sec
	Sequential Write	8 MB/sec

NOTE: The sleep-to-write and sleep-to-read times are the times it takes the card to exit sleep mode when any command is issued by the host to when the card is reading or writing. TRS* Tele-Radio-Space GmbH Standard ATA CF-Cards do not require a reset to exit sleep mode. See Section 1.7.5.

2.4 System Reliability

Table 2.4 Reliability

MTBF (@ 25°C)	>2 500 000 hours
Preventive Maintenance	None
Data Reliability	<1 non-recoverable error in 10^{14} bits read <1 erroneous correction in 10^{20} bits read
Endurance: **- Standard Temperature** **- Extended Temperature**	 >2 000 000 erase/program cycles >2 000 000 erase/program cycles

2.5 Physical Specifications

The following sections provide the physical specifications for CompactFlash Cards.

Refer to Table 2.5 and see Figure 2.5 for CompactFlash Memory Card physical specifications and dimensions.

Table 2.5 CompactFlash Physical Specifications

	CompactFlash
Weight:	11.4 g (.40 oz) typical, 14.2 g (.50 oz) maximum
Length:	36.40 ± 0.15 mm (1.433 ±.006 in)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in)
Thickness:	3.3 mm ± 0.10 mm (.130 ±.004 in) (Excluding Lip)

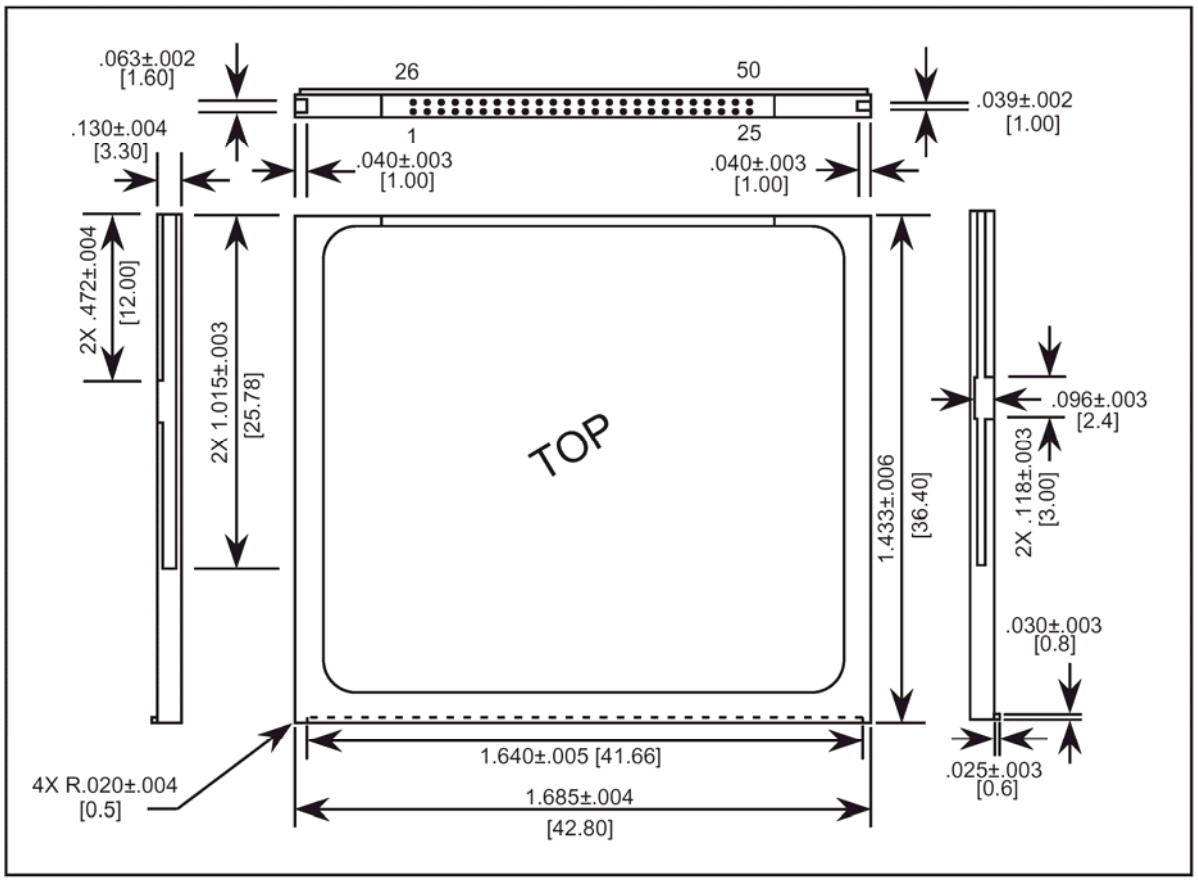


Figure 2.5 CompactFlash Memory Card Dimensions

2.6 Capacity Specifications

Table 2.6 shows the specific capacity for the various model.

Table 2.6 Model Capacities

Model No.	Capacity	Flash Chip	Total	Controller	
STAR CFI-016Mx201.yyy.zz	16MB	128MB	1	F2	Standard
STAR CFI-032Mx202.yyy.zz	32MB	128MB	2	F2	Standard
STAR CFI-032Mx211.yyy.zz	32MB	256MB	1	F2	Standard
STAR CFI-048Mx203.yyy.zz	48MB	128MB	3	F2	Ask Sales
STAR CFI-064Mx204.yyy.zz	64MB	128MB	4	F2	Standard
STAR CFI-064Mx212.yyy.zz	64MB	256MB	2	F2	Standard
STAR CFI-064Mx221.yyy.zz	64MB	512MB	1	F2	Standard
STAR CFI-096Mx213.yyy.zz	96MB	256MB	3	F2	Ask Sales
STAR CFI-128Mx214.yyy.zz	128MB	256MB	4	F2	Standard
STAR CFI-128Mx222.yyy.zz	128MB	512MB	2	F2	Standard
STAR CFI-128Mx231.yyy.zz	128MB	1GB	1	F2	Standard
STAR CFI-192Mx223.yyy.zz	192MB	512MB	3	F2	Ask Sales
STAR CFI-256Mx224.yyy.zz	256MB	512MB	4	F2	Standard
STAR CFI-256Mx232.yyy.zz	256MB	1GB	2	F2	Standard
STAR CFI-256Mx241.yyy.zz	256MB	2GB	1	F2	Standard
STAR CFI-384Mx233.yyy.zz	384MB	1GB	3	F2	Ask Sales
STAR CFI-512Mx234.yyy.zz	512MB	1GB	4	F2	Standard
STAR CFI-512Mx242.yyy.zz	512MB	2GB	2	F2	Standard
STAR CFI-512Mx251.yyy.zz	512MB	4GB	1	F2	Standard
STAR CFI-768Mx243.yyy.zz	768MB	2GB	3	F2	Ask Sales
STAR CFI-001Gx244.yyy.zz	1GB	2GB	4	F2	Standard
STAR CFI-001Gx252.yyy.zz	1GB	4GB	2	F2	Standard
STAR CFI-001Gx361.yyy.zz	1GB	8GB	1	F2	Standard
STAR CFI-01G5x254.yyy.zz	1,5GB	4GB	3	F2	Ask Sales
STAR CFI-002Gx254.yyy.zz	2GB	4GB	4	F2	Standard
STAR CFI-002Gx362.yyy.zz	2GB	8GB	2	F2	Standard
STAR CFI-002Gx371.yyy.zz	2GB	16GB	1	F2	Standard
STAR CFI-003Gx363.yyy.zz	3GB	8GB	3	F2	Ask Sales
STAR CFI-004Gx364.yyy.zz	4GB	8GB	4	F2	Standard
STAR CFI-004Gx372.yyy.zz	4GB	16GB	2	F2	Standard
STAR CFI-006Gx373.yyy.zz	6GB	16GB	3	F2	Ask Sales
STAR CFI-008Gx374.yyy.zz	8GB	16GB	4	F2	Standard

NOTE: x = **S** Standard Temperature 0°C – +65°C; **I** Industrial Temperature -40°C – +80°C
y = Different types of revisions
z = Different types of options

Please, refer the “Ordering Information” under section 7

3. Interface Description

The following sections provide detailed information on the Standard ATA product interface.

3.1 CF Card Pin Assigments and Pin Type

The signal/pin assignments are listed in Table 3.1 Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

Table 3.1 CompactFlash Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Name	Signal Name	Pin Type	In, Out[4] Type	Pin Name	Signal Name	Pin Type	In, Out[4] Type	Pin Name	Signal Name	Pin Type	In, Out[4] Type
1	GND	PWR	Ground	1	GND	PWR	Ground	1	GND	PWR	Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I2U	7	-CE1	I	I2U	7	-CE1	I	I2U
8	A10	I	I1Z	8	A10	I	I1Z	8	A10	I	I1Z
9	-OE	I	I2U	9	-OE	I	I2U	9	-OE	I	I2U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07	I	I1Z
13	VCC	PWR	Power	13	VCC	PWR	Power	13	VCC	PWR	Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	OT3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I2U	32	-CE2[1]	I	I2U	32	-CE2[1]	I	I2U
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I2U	34	-IORD	I	I2U	34	-IORD	I	I2U
35	-IOWR	I	I2U	35	-IOWR	I	I2U	35	-IOWR	I	I2U
36	-WE	I	I2U	36	-WE	I	I2U	36	-WE	I	I2U
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OT1
38	VCC	PWR	Power	38	VCC	PWR	Power	38	VCC	PWR	Power
39	-CSEL	I	I2Z	39	-CSEL	I	I2Z	39	-CSEL	I	I2Z
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY	O	OT1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	DMARQ[5]	O	OT1
44	-REG	I	I2U	44	-REG	I	I2U	44	-DMACK[5]	I	I2U
45	BVD2	I/O	I1U,OT1	45	-SPKR	I/O	I1U,OT1	45	-DASP	I/O	I1U,OT1
46	BVD1	I/O	I1U,OT1	46	-STSCHG	I/O	I1U,OT1	46	-PDIAG	I/O	I1U,OT1

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Name	Signal Name	Pin Type	In, Out[4] Type	Pin Name	Signal Name	Pin Type	In, Out[4] Type	Pin Name	Signal Name	Pin Type	In, Out[4] Type
47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3
50	GND	PWR	Ground	50	GND	PWR	Ground	50	GND	PWR	Ground

NOTE: 1 These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. Refer to Section 3.3 for definitions of In, Out type.
5. CompactFlash products support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

3.2 Electrical Description

The TRS* CompactFlash Cards are optimized for operation with hosts that support the PCMCIA I/O interface standard conforming to the PC Card ATA specification. However, the CompactFlash Cards may also be configured to operate in systems that support only the memory interface standard. The configuration of the CompactFlash Cards are controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the CompactFlash Memory Card.

Table 3.2 describes the I/O signals. Signals are designated as inputs when their source is the host, while signals that the CompactFlash Memory Card sources are outputs. The CompactFlash Card logic levels conform to those specified in the *PCMCIA Release 2.1 Specification*. See Section 3.3 for definitions of Input and Output type.

Table 3.2 Signal Description

Signal Name	Dir.	Description
A10—A0 (PC Card Memory Mode)	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10—A0 (PC Card I/O Mode)		This signal is the same as the PC Card Memory Mode signal.
A2—A0 (True IDE Mode) A10—A3 (True IDE Mode)		In True IDE Mode only A[2:0] is used to select the one of eight registers in the Task File. In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed		This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)		In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.

Signal Name	Dir.	Description
BVD2 (PC Card Memory Mode)	I/O	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)		This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)		In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	These Card Detect pins are connected to ground on the CompactFlash Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)		This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)		This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 3-11, 3-12, 3-15, and 3-16.
-CE1, -CE2 (PC Card I/O Mode) Card Enable		This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)		In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode).	I	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)		This signal is not used for this mode.
-CSEL (True IDE Mode)		This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D00—D15 (PC Card Memory Mode)	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D00—D15 (PC Card I/O Mode)		These signals are the same as the PC Card Memory Mode signal.
D00—D15 (True IDE Mode)		In True IDE Mode all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND (PC Card Memory Mode)	PWR	Ground. This signal is the same for all modes.
GND (PC Card I/O Mode)		Ground. This signal is the same for all modes.
GND (True IDE Mode)		Ground. This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge		The Input Acknowledge signal is asserted by the CompactFlash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
DMARQ1 (True IDE Mode)		This signal is used for DMA data transfers between host and device and is asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- (i.e., the device waits until the host asserts DMACK- before negating DMARQ, and reasserting DMARQ if there is more data to transfer).

Signal Name	Dir.	Description
-IORD (PC Card Memory Mode)	I	This signal is not used in this mode.
-IORD (PC Card I/O Mode)		This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)		In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)		The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)		In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)		In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)		To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	In Memory Mode this signal is set high when the CompactFlash Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)		I/O Operation—After the CompactFlash Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)		In True IDE Mode, this signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)		The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK1 (True IDE Mode)		This signal is used by the host in response to DMARQ to initiate DMA transfers. **NOTE**: This signal may be negated by the host to suspend the DMS transfer in process. For Multiword DMA transfers, the device may negate DMARQ with the tL specified time once the -DMACK is asserted and reasserted again at a later time to resume DMA operation. Alternatively, if the device is able to continue the data transfer, the device may leave DMARQ asserted and wait for the host to reassert -DMACK.
RESET (PC Card Memory Mode)	I	When the pin is high, this signal resets the CompactFlash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)		This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)		In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	PWR	+5 V, +3.3 V power. This signal is the same for all modes.
VCC (PC Card I/O Mode)		+5 V, +3.3 V power. This signal is the same for all modes.
VCC (True IDE Mode)		+5 V, +3.3 V power. This signal is the same for all modes.

Signal Name	Dir.	Description
-VS1 -VS2 (PC Card Memory Mode)	O	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is open and reserved by PC Card for a secondary voltage. This signal is the same for all modes.
-VS1 -VS2 (PC Card I/O Mode)		Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is open and reserved by PC Card for a secondary voltage. This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)		Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is open and reserved by PC Card for a secondary voltage. This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	TRS Star Cards do not assert the -**WAIT** signal.
-WAIT (PC Card I/O Mode)		TRS Star Cards do not assert the -**WAIT** signal.
-IORDY (True IDE Mode)		TRS Star Cards supported the -**IORDY** signal.
-WE (PC Card Memory Mode)	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)		In PC Card I/O Mode, this signal is used for writing the configuration registers.
Reserved (True IDE Mode)		In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect	O	Memory Mode—The CompactFlash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)		I/O Operation—When the CompactFlash Card is configured for I/O Operation, Pin 24 is used for the - I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)		In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

1 CompactFlash products support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

3.3 Electrical Specification

The following table defines all D.C. Characteristics for the TRS Star CompactFlash Card Series. Unless otherwise stated, conditions are:

Table 3.3 D.C Characteristics

TRS* STAR CFI-xxxMSyy.zzz	TRS* STAR CFI-xxxMIyy.zzz
Vcc = 5V ±10% Vcc = 3.3V ± 10% Ta = 0°C to 65°C	Vcc = 5V ±10% Vcc = 3.3V ± 10% Ta = -40°C to 80°C
Absolute Maximum conditions are: Vcc = -0.3V min. to 7.0V max. V* = -0.5V min. to Vcc + 0.5V max.	

NOTE: * Voltage on any pin except Vcc with respect to GND.

3.3.1 Input Leakage Control

NOTE: In Table 3.3.1 "x" refers to the characteristics described in Section 3.3.2. For example, 1U indicates a pull up resistor with a type 1 input characteristic.

Table 3.3.1 Input Leakage Control

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
IxZ	Input Leakage Current	IL	Vih = Vcc/Vil = Gnd	-1		1	µA
IxU	IxU Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

NOTE: The minimum pullup resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the CompactFlash Memory Card Series product to reduce power use.

3.3.2 Input Characteristics

Table 3.3.2 Input Characteristics

Type	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
			VCC = 3.3V ±10%			VCC = 5.0V ±10%			
1	Input Voltage CMOS	Vih Vil	1.8		0.6	2.6		0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.4		0.8	Volts

3.3.3 Output Drive Type

In Table 3.3.3, "x" refers to the characteristics described in Section 3.3.4. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Table 3.3.3. Output Drive Type

Type	Output Type	Valid Conditiones
OTx	Totempole	Ich and Iol
OZx	Tri-State N-P Channel	Ioh and Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

3.3.4 Output Drive Characteristics

Table 3.3.4 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		GND +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		GND +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		GND +0.4V	Volts
X	Tri-State Leakage Current	Loz	Vol = Gnd Voh = Vcc	-10		10	µA

3.3.5 Power-up/Power-down Timing

The timing specification in Table 3.3.5 was defined to retain data in the SRAM Card during power-up or power-down cycles and to permit peripheral cards to perform power-up initialization.

Table 3.3.5 Power-up/Power-down Timing

Item	Symbol	Condition	Value		
			Min	Max	Unit
CE signal level[1]	Vi (CE)	0V <VCC <2.0V	0	ViMAX	V
		2.0V <VCC <VIH	<VCC – 0.1	ViMAX	V
		<VIH <VCC	Vih	ViMAX	V
CE Setup Time	Tsu (VCC)		20		ms
CE Setup Time	Tsu (RESET)		20		ms
CE Recover Time	Trec (VCC)		0.001		ms
VCC Rising Time[2]	Tpf	10% 90% of (VCC + 5%)	0.1	300	ms
VCC Rising Time[2]	tpf	90% of (VCC - 5%) 10%	3.0	300	ms
Reset Width	Tw (RESET)		10		µs
	Th (Hi-z Reset)		1		ms
	Ts (Hi-z Reset)		0		ms

1. ViMAX means Absolute Maximum Voltage for Input in the period of 0V <VCC <2.0V, Vi (CE) is only 0V~ViMAX.
2. The tpr and tpf are defined as “linear waveform” in the period of 10% to 90% or vice-versa. Even if the waveform is not“linear waveform,” its rising and falling time must be met by this specification.

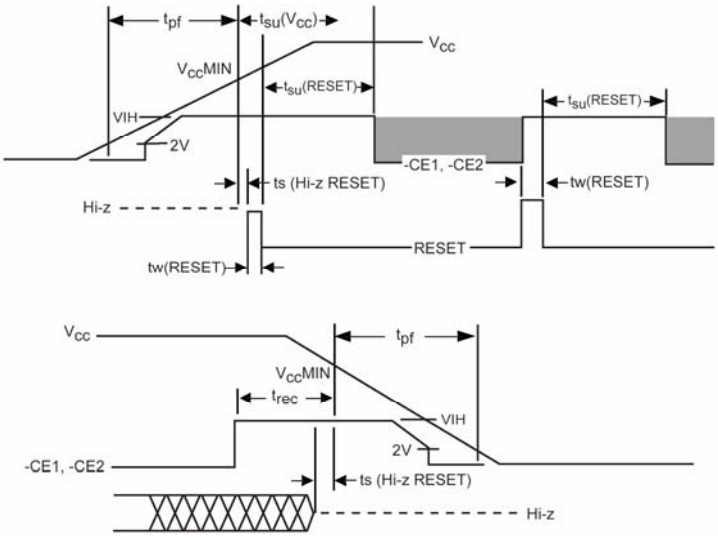


Figure 3.3.5-1 Power-Up/Power-Down Timing for Systems Supporting RESET

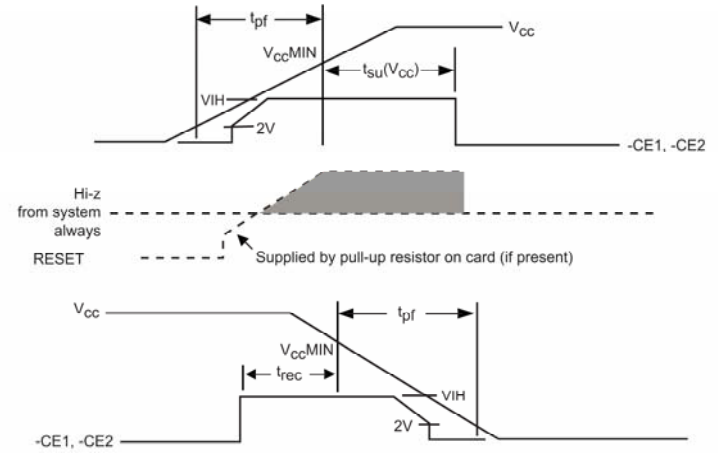


Figure 3.3.5-2 Power-Up/Power-Down Timing for Systems Not Supporting RESET

3.3.6 Common Memory Read Timing

Table 3.3.6 Common Memory Read Timing Specification for all Types of Memory

Speed Version term	Symbol	IEEE Symbol	100 ns	
			Min	Max
Read Cycle Time	tc(R)	tAVAV	100	
Address Access Time[1]	ta(A)	tAVQV		100
Card Enable Access Time	ta(CE)	tELQV		100
Output Enable Access Time	ta(OE)	tGLQV		50
Output Disable Time from -**OE**	tdis(OE)	tGHQZ		50
Output Disable Time from -**CE**	tdis(CE)	tEHQZ		50
Output Enable Time from -**CE**	ten(CE)	tELQNZ	5	
Output Enable Time from -**OE**	ten(OE)	tGLQNZ	5	
Data Valid from Add Change[1]	tv(A)	tAXQX	0	
Address Setup Time	tsu (A)	tAVGL	10	
Address Hold Time	th (A)	tGHAX	15	
Card Enable Setup Time	tsu (CE)	tELGL	0	
Card Enable Hold Time	th (CE)	tGHEH	15	

1. The -**REG** signal timing is identical to address signal timing.

NOTE: All timings measured at the card. Skews and delays from the system driver/receiver to the card must backcounted for by the system.

3.3.7 Common and Attribute Memory Write Timing

The write timing specifications for Common and Attribute memory are the same.

Table 3.3.7 Common and Attribute Memory Write Timing Specifications

Speed Version term	Symbol	IEEE Symbol	100 ns	
			Min	Max
Write Cycle Time	tc(W)	tAVAV	100	
Write Pulse Width	tw(WE)	tWLWH	60	
Address Setup Time[1]	tsu(A)	tAVWL	10	
Address Setup Time for -**WE**[1]	tsu(A-WEH)	tAVWH	70	
Card Enable Setup Time for -**WE**	tsu(CE-WEH)	tELWH	70	
Data Setup Time from -**WE**	tsu(D-WEH)	tDVWH	40	
Data Hold Time	th(D)	tWMDX	15	
Write Recover Time	trec(WE)	tWMAX	15	
Output Disable Time from -**WE**	tdis(WE)	tWLQZ		50
Output Disable Time from -**OE**	tdis(OE)	tGHQZ		50
Output Enable Time from -**WE**	ten(WE)	tWHQNZ	5	
Output Enable Time from -**OE**	ten(OE)	tGLQNZ	5	
Output Enable Setup from -**WE**	tsu(OE-WE)	tGHWL	10	
Output Enable Hold from -**WE**	th(OE-WE)	tWHGL	10	
Card Enable Setup Time	tsu (CE)	tELWL	0	
Card Enable Hold Time	th (CE)	tGHEH	15	

1. The -**REG** signal timing is identical to address signal timing.

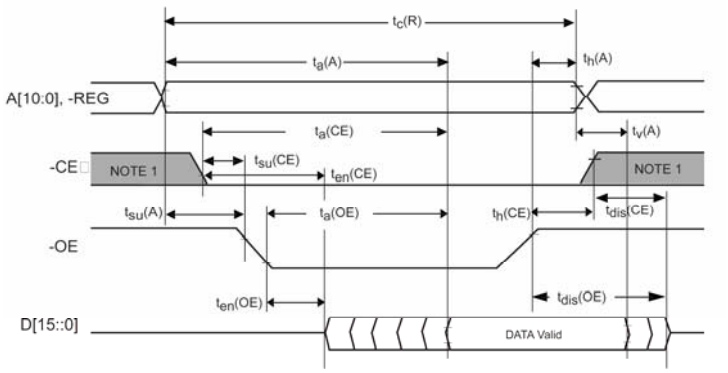
NOTE: All timings measured at the card. Skews and delays from the system driver/receiver to the card must backcounted for by the system.

3.3.8 Attribute Memory Read Timing Specification

Table 3.3.8 Attribute Memory Read Timing Specification for all Types of Memory

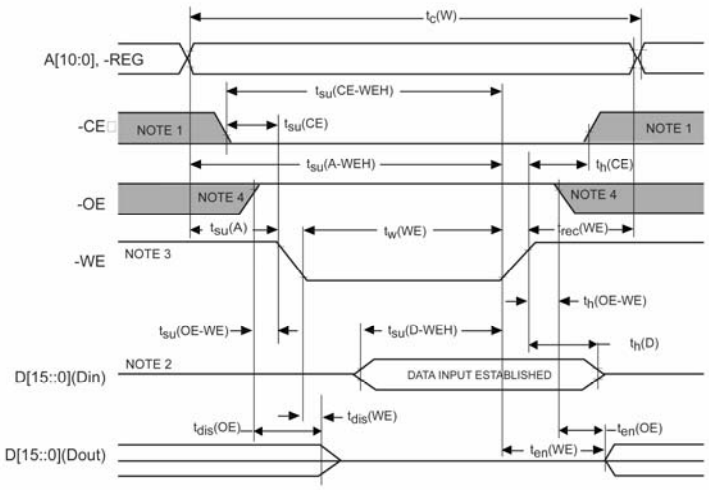
Speed Version term	Symbol	IEEE Symbol	300 ns	
			Min	Max
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from -**OE**	tdis(OE)	tGHQZ		100
Output Enable Time from -**OE**	ten(OE)	tGLQNZ	5	
Data Valid from Add Change	tv(A)	tAXQX	0	
Address Setup Time	tsu (A)	tAVGL	30	
Address Hold Time	th (A)	tGHAX	20	
Card Enable Setup Time	tsu (CE)	tELGL	0	
Card Enable Hold Time	th (CE)	tGHEH	20	

3.3.9 Memory Timing Diagramm



1. Shaded areas may be high or low.
2. TRS* Tele-Radio-Space GmbH cards do not assert the -**WAIT** signal.

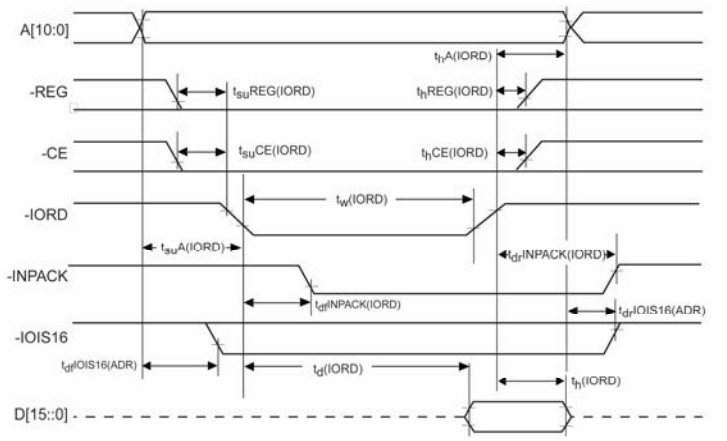
Figure 3.3.9-1 Common and Attribute Memory Read Timing Diagram



1. Shaded areas may be high or low.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (**D[15::0]**) by the host system
3. May be high or low for write timing, but restrictions on -**OE** from previous figures apply.
4. TRS* Tele-Radio-Space GmbH cards do not assert the -**WAIT** signal.

Figure 3.3.9-2 Common and Attribute Memory Write Timing Diagram

3.3.10 I/O Read (Input) Timing Specification



1. All timings are measured at the card.
2. Skews and delays from the host system driver/receiver to the card must be accounted for by the system design.
3. **D[15::0]** signifies data provided by the card to the host system.

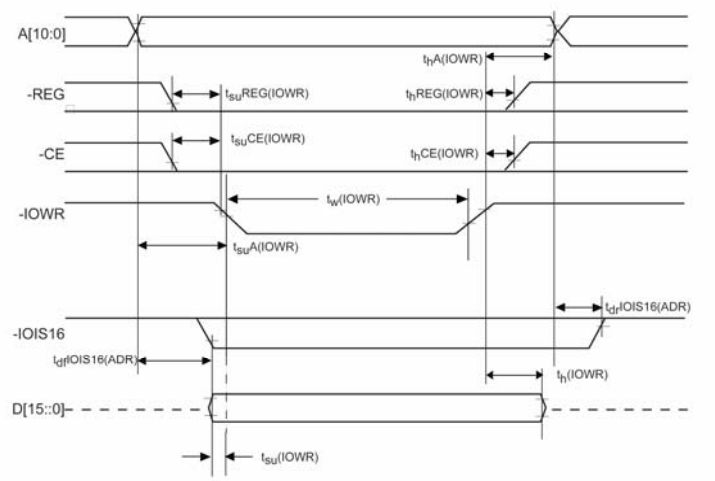
Figure 3.3.10 I/O Read Timing Diagram

Table 3.3.10 I/O Read (Input) Timing Specification

Speed Version term	Symbol	IEEE Symbol	ns	
			Min	Max
Data Delay after **-IORD**	td(IORD)	tIGLQV		100
Data Hold following **-IORD**	th(IORD)	tIGHQX	0	
-IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before **-IORD**	tsuA(IORD)	tAVIGL	70	
Address Hold following **-IORD**	thA(IORD)	tIGHAX	20	
-CE Setup before **-IORD**	tsuCE(IORD)	tELIGL	5	
-CE Hold following **-IORD**	thCE(IORD)	tIGHEH	20	
-REG Setup before **-IORD**	tsuREG(IORD)	tRGLIGL	5	
-REG Hold following **-IORD**	thREG(IORD)	tIGHRGH	0	
-INPACK Delay Falling from **-IORD**	tdfINPACK(IORD)	tIGLIAL	0	45
-INPACK Delay Rising from **-IORD**	tdrINPACK(IORD)	tIGHIAH		45
-IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

The maximum load on **-INPACK** and **-IOIS16** is 1 LSTTL with 50 pF total load.

3.3.11 I/O Write (Output) Timing Specification



1. All timings are measured at the card.
2. Skews and delays from the host system driver/receiver to the card must be accounted for by the system design.
3. **D[15::0]** signifies data provided by the host system to the card.

Figure 3.3.11 I/O Write Timing Diagram

Table 3.3.11 I/O Write Timing Specification

Speed Version term	Symbol	IEEE Symbol	ns	
			Min	Max
Data Setup before **-IOWR**	tsu(IOWR)	tDVIWL	60	
Data Hold following **-IOWR**	th(IOWR)	tIWHDX	30	
-IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before **-IOWR**	tsuA(IOWR)	tAVIWL	70	
Address Hold following **-IOWR**	thA(IOWR)	tIWHAX	20	
-CE Setup before **-IOWR**	tsuCE(IOWR)	tELIWL	5	
-CE Hold following **-IOWR**	thCE(IOWR)	tIWHEH	20	
-REG Setup before **-IOWR**	tsuREG(IOWR)	tRGLIWL	5	
-REG Hold following **-IOWR**	thREG(IOWR)	tIWHRGH	0	
-IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

The maximum load on **-IOIS16** is 1 LSTTL with 50 pF total load.

3.3.12 True IDE Mode

The following sections provide valuable information for the True IDE mode.

3.3.12.1 De-skewing

The host shall provide cable de-skewing for all signals originating from the device. The device shall provide cable de-skewing for all signals originating at the host.
All timing values and diagrams are shown and measured at the connector of the selected device.

3.3.12.2 PIO Transfer Timing

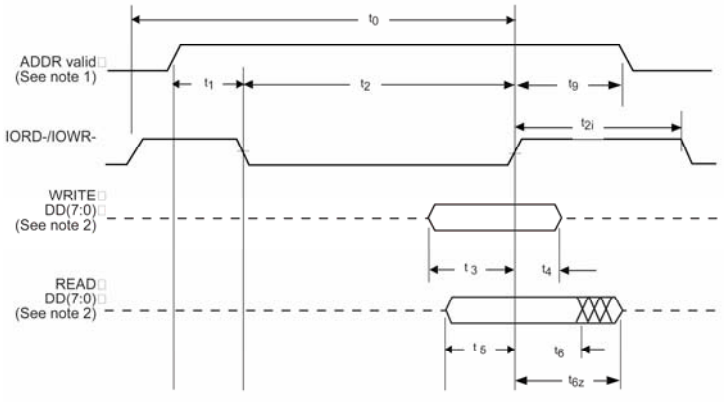
The minimum cycle time supported by Standard-Grade devices in PIO mode 4 and Multiword DMA mode 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated mode.

Register Transfers

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list. In Table 3-15, t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements are greater than the sum of t2 and t2i. This means a host implementation may lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

The *IORD-data tri-state* parameter specifies the time from the negation edge of /IORD to the time that the data bus is no longer driven by the device (tri-state).

Table 3.3.12.2 defines the minimum value that shall be placed in word 68.



1. Device address consists of signals **-CS0**, **-CS1** and **-DA(2:0)**.
2. Data consists of DD(7:0).

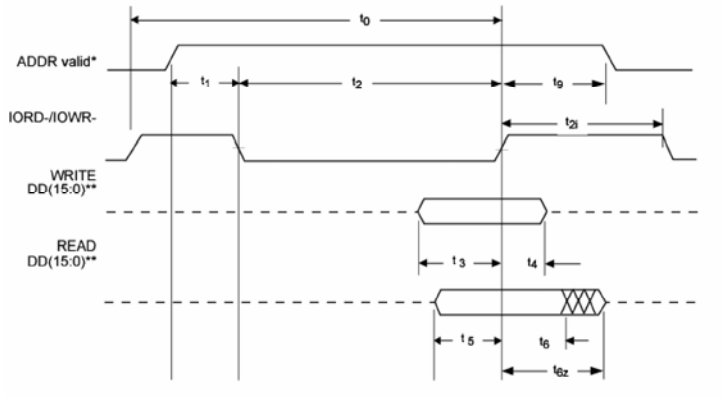
Figure 3.3.12.2-1 Register Transfer To/From Device

In Table 3.3.12.2-1, t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements are greater than the sum of t2 and t2i. This means a host implementation may lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
The *IORD-data tri-state* parameter specifies the time from the negation edge of /IORD to the time that the data bus is no longer driven by the device (tri-state).

Table 3.3.12.2-1 Register Transfer To/From Device

PIO Timing Parameter			Mode 1 (ns)	Mode 4 (ns)	Note
t0	Cycle time	{min}	383	120	
t1	Address valid to IORD-/IOWR- setup	{min}	50	25	
t2	IORD-/IOWR- pulse width 8-bit	{min}	290	70	
t2i	IORD-/IOWR- recovery time	{min}	-	25	
t3	IOWR- data setup	{min}	45	20	
t4	IOWR- data hold	{min}	20	10	
t5	IORD- data setup	{min}	35	20	
t6	IORD- data hold	{min}	5	5	
t6z	IORD- data tri-state	{max}	30	30	
t9	IORD-/IOWR- to address valid hold	{min}	15	10	

PIO Data Transfers
Figure 3.3.12.2-2 defines the relationships between the interface signals for PIO data transfers. For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list. The information that prefaces Table 3-15 also pertains to Table 3-16 below.



* Device address consists of signals –CS0, -CS1 and –DA(2:0)
** Data Consists of DD(0:15)

Figure 3.3.12.2-2 PIO Data Transfer To/From Device

Table 3.3.12.2-2 PIO Data Transfer To/From Device

PIO Timing Parameter			Mode 1 (ns)	Mode 4 (ns)	Note
t0	Cycle time	{min}	383	120	
t1	Address valid to IORD-/IOWR- setup	{min}	50	25	
t2	IORD-/IOWR- pulse width 8-bit	{min}	125	70	
t2i	IORD-/IOWR- recovery time	{min}	-	25	
t3	IOWR- data setup	{min}	45	20	
t4	IOWR- data hold	{min}	20	10	
t5	IORD- data setup	{min}	35	20	
t6	IORD- data hold	{min}	5	5	
t6z	IORD- data tri-state	{max}	30	30	
t9	IORD-/IOWR- to address valid hold	{min}	15	10	

3.3.12.3 Multiword DMA Date Transfer Timing

TRS Star CompactFlash Card support Multiword DMA operation in IDE mode (see Figure 3.3.12.3). The timings associated with Multiword DMA Transfers are defined in Table 3.4-1. CompactFlash products now support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

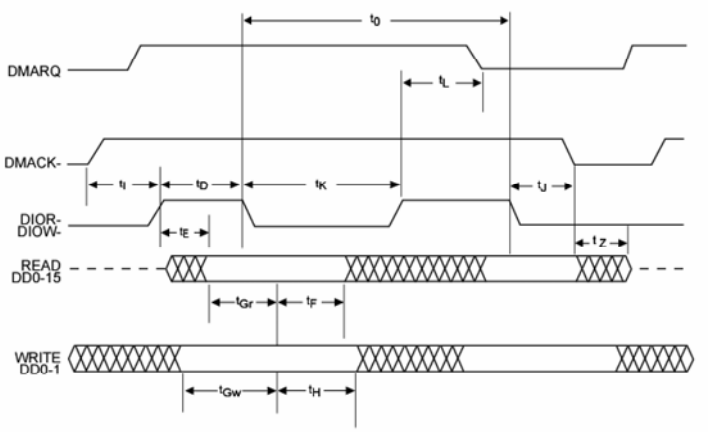


Figure 3.3.12.3 Multiword DMA Transfer

In Table 3.3.12.3, t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements are greater than the sum of t2 and t2i. This means a host implementation may lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

The *IORD-data tri-state* parameter specifies the time from the negation edge of /IORD to the time that the data bus is no longer driven by the device (tri-state).

Table 3.3.12.3 Multiword DMA Data Transfer Timing Specifications

Multiword DMA Timing Parameters		Mode 0 (ns)		Mode 2 (ns)		Notes
		Min	Max	Min	Max	
t0	Cycletime	480		120		1
tC	DMACKtoDMARQdelay		-		-	
tD	DIOR-/DIOW-16-bit	215		70		1
tE	DIOR-dataacess		150		-	
tF	DIOR-datahold	5		5		
tG	DIOW-datasetup	100		20	n/a	
tG	DIOW-datasetup	100		20		
tH	DIOW-datahold	20		10		
tI	DMACK to DIOR-/DIOW-setup	0		0		
tJ	DIOR-/DIOW-toDMACKhold	20		5		
tKr	DIOR-negated pulsewidth	50		25		1
tKw	DIOW-negated pulsewidth	215		25		1
tLr	DIOR- to DMARQdelay		120		35	
tLw	DIOW- to DMARQdelay		40		35	
tZ	DMACK- to tristate		20		35	

3.4 Card Configuration

The CompactFlash Memory Cards are identified by appropriate information in the Card Information Structure (CIS). The configuration registers in Table 3.4-1 and Table 3.4-2 are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 3.4-1 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table 3.4-2 Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-4	A3	A2	A1	A0	Selected Register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the CompactFlash Memory Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

3.4.1 Attribute Memory Funktion

Attribute memory is a space where CompactFlash Memory Card identification and configuration information is stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 3.4.1 for signal states and bus validity for the Attribute Memory function.

Table 3.4.1 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-8	D7-0
Standby Mode	X	H	L	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) {Invalid}	L	H	L	L	L	H	L	Not care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Not care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) {Invalid}	L	L	L	L	X	H	L	Not care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Not care	Even Byte

NOTE: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

3.4.2 Configuration Option Register (Addr. 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Memory Card.

Table 3.4.2-1 Configuration Option Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset—Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Memory Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Memory Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PC Card Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5—Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the CompactFlash Memory Card as shown below.

NOTE: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 3.4.2-2 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

3.4.3 Card Configuration and Status Register (Addr. 202h in Attribute Memory)

The Card Configuration and Status Register contain information about the Card's condition.

Table 3.4.3. Card Configuration and Status Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Memory Card is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the CompactFlash Memory Card is configured for I/O.

IOis8 The host sets this bit to a one (1) if the CompactFlash Memory Card is to be configured in an 8-bit I/O mode. The CompactFlash Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the CompactFlash Memory Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Card enters a power down mode. When zero (0), the host is requesting the CompactFlash Card to enter the active mode. The PC Card Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The CompactFlash Card automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

3.4.4 Pin Replacement Register (Address 204h in Attribute Memory)

Table 3.4.4-1. Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	RRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RRdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

RWProt This bit is always zero (0) since the CompactFlash Memory Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 3.4.4-2 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
O	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

3.4.5 Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Table 3.4.5 Socket and Copy Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #(0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the CompactFlash Memory Card.

3.5 I/O Transfer Function

The I/O transfer to or from the CompactFlash Memory Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16-bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The CompactFlash Card permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Card responds (refer to Table 3.5).

Table 3.5 I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-8	D7-0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Do not care Do not care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Do not care	Do not care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Do not care

3.6 Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash or PCMCIA card can be either 8 or 16 bits. The CompactFlash or PCMCIA cards permit both 8- and 16-bit accesses to all of its Common addresses (refer to Table 3.6).

Table 3.6 Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-IOE	-WE	D15-8	D7-0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H H	H H	L L	L L	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L L	H H	L L	Do not care Do not care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Do not care

3.7 True IDE Mode I/O Transfer Function

The CompactFlash or PCMCIA card can be configured in a True IDE Mode of operation. This CompactFlash or PCMCIA card is configured in this mode only when the -OE input signal is grounded by the host when power is applied to the card. In True IDE Mode, the PC Card protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In addition, No Memory or Attribute Registers are accessible to the host. TRS* Tele-Radio-Space GmbH products permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8-bit Mode.

NOTE: Removing and reinserting the CompactFlash Memory Card while the host computer's power is on will reconfigure the CompactFlash Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Card in True IDE Mode, the 50-pin socket must be power cycled with the CompactFlash Card inserted and -OE (output enable) grounded by the host.

Table 3.7, on the next page, defines the function of the operations for the True IDE Mode.

Table 3.7 IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-8	D7-0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

4. ATA Drive Register Set Definition and Protocol

The CompactFlash Memory Card can be configured as a high performance I/O device through the following ways:

- Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16-byte I/O block using any available IRQ.
- Memory space.

The communication to or from the CompactFlash Memory Card is done using the Task File registers, which provide all the necessary registers for control and status information. The PC Card interface connects peripherals to the host using four register mapping methods. Table 4 is a detailed description of these methods.

Table 4 I/O Configurations

Standard Configurations				
Config Index	**IO or Memory**	**Address**	**Drive #**	**Description**
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

4.1 I/O Primary and Secondary Address Configurations

Table 4.1 Primary and Secondary I/O Decoding

-REG	A9-4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
2. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

4.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Memory Card, the registers are accessed in the block of I/O space decoded by the system in Table 4.2

Table 4.2 Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Note
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

NOTES: 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines that are not indicated are ignored by the CompactFlash Memory Card for accessing all the registers in this table.

4.3 Memory Mapped Addressing

When the CompactFlash Memory Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as shown in Table 4.3

Table 4.3 Memory Mapped Decoding

-REG	A10	A9-4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

NOTES:
1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.
2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash Memory Card.

4.4 True IDE Mode Addressing

When the CompactFlash Memory Card is configured in the True IDE Mode the I/O decoding is as listed in Table 4-5.

Table 4.4 True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

4.5 ATA Register

NOTE: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

4.5.1 Data Register (Address – 1F0[170]; Offset 0, 8, 9)

The Data Register is a 16-bit register, and it is used to transfer data blocks between the Standard ATA product data buffer and the Host. This register overlaps the Error Register. Table 4-6 describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

NOTE: Because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. TRS* Tele-Radio-Space GmbH products treat these accesses as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Table 4-.5.1 Data Register

Data Register	-CE2	-CE1	A0	Offset	Data Bus
Word Data Register	0	0	X	0, 8, 9	D15-D00
Even Data Register	1	0	0	0, 8	D07-D00
Odd Data Register	1	0	1	9	D07-D00
Odd Data Register	0	1	X	8, 9	D15-D08
Error/Feature Register	1	0	1	1, Dh	D07-D00
Error/Feature Register	0	1	X	1	D15-D08
Error/Feature Register	0	0	X	Dh	D15-D08

4.5.2 Error Register (Address – 1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

Table 4.5.2 Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.5.3 Feature Register (Address – 1F1[171]; Offset 1, 0Dh Read Only)

This register provides information regarding features of the Standard ATA product that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high (except in True IDE Mode operation).

4.5.4 Sector Count Register (Address – 1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Memory Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.5.5 Sector Number (LBA 7-0) Register (Address – 1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Memory Card data access for the subsequent command.

4.5.6 Cylinder Low (LBA 15-8) Register (Address – 1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.5.7 Cylinder High (LBA 23-16) Register (Address – 1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.5.8 Drive/Head (LBA 27-24) Register (Address – 1F6[176]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

Table 4.5.8 Drive/Head

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected When DRV=1, drive (card) 1 is selected. In PCMCIA Mode operation, Card 0 or 1 is selected using the copy field of the PC Card Socket and Copy configuration register.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.5.9 Status, Alternate Status Reg. (Addr. – 1F7[177]&3F6[376]; Offset 7&Eh)

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

Table 4.5.9 Status Alternate Register

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the Standard ATA product has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the Standard ATA product is ready to accept a command.
Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC) This bit is set when the Standard ATA product is ready.
Bit 3 (DRQ) The Data Request is set when the Standard ATA product requires that information be transferred either to or from the host through the Data register.
Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX) This bit is always set to 0.
Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.5.10 Device Control Register (Address – 3F6[376]; Offset Eh)

This register is used to control the card interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

Table 4.5.10 Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (Do not care).
Bit 6 This bit is an X (Do not care).
Bit 5 This bit is an X (Do not care).
Bit 4 This bit is an X (Do not care).
Bit 3 This bit is ignored by the card.
Bit 2 (SW Rst) This bit is set to 1 in order to force the card to perform an AT Disk controller Soft Reset operation. This does not change the PC Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The card remains in Reset until this bit is reset to '0'.
Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.
Bit 0 This bit is ignored by the card.

4.5.11 Card (Drive) Address Register (Address – 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

Table 4.5.11 Card (Drive) Register

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the Standard ATA product. Following are some possible solutions to this problem for the PC Card implementation:

1. Locate the Standard ATA product at a non-conflicting address (i.e., Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and an Standard ATA product in the system at the same time.

3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when an Standard ATA product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.

4. Do not use the Standard ATA product's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the Standard ATA product or b) if provided use an additional Primary/Secondary configuration in the Standard ATA product that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

5. ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the Standard ATA products. Commands are issued by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 5.1) of command acceptance, all dependent on the host not issuing commands unless the card is not busy. (The BUSY bit in the status and alternate status registers is 0.)

- Upon receipt of a Class 1 command, the card sets the BUSY bit within 400 nsec.
- Upon receipt of a Class 2 command, the CompactFlash Memory Card sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears the BUSY bit within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the CompactFlash Memory Card sets the BUSY bit within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no reassignments), and clears the BUSY bit within 400 nsec of setting DRQ.

5.1 ATA Command Set

Table 5-1 summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 5.1 ATA Command Set

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	-	-
1	Erase Sector(s) (Note 2)	C0h	-	Y	Y	Y	Y	Y
2	2 Format Track	50h	-	Y		Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8 or C9	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense (Note 1)	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Stand By	E2h or 96h	-	-	-	-	D	-
1	Stand By Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector (Note 1)	87h	-	Y	Y	Y	Y	Y
1	Wear Level (Note 1)	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CA or CB	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Long Sector	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase (Note 2)	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase (Note 2)	38h	-	Y	Y	Y	Y	Y
2	Write Verify Sector(s)	3Ch	-	Y	Y	Y	Y	Y

Note 1: These commands are not standard ATA commands but provide additional functionality.

Note 2: These commands are not standard ATA commands and these features are no longer supported with the introduction of 256 Mbit Flash Technology. If one of these commands is issued, the sectors will be erased but there will be no net gain in write performance when using the Write Without Erase command.

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use). Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Card and head parameters are used; D—only the CompactFlash Card parameter is valid and not the head parameter.

5.1.1 Check Power Mode – 98h, E5h

The Check Power Mode command in Table 5.1.1 checks the power mode.

Table 5.1.1 Check Power Mode

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E5h or 98h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

If the card is in, going to, or recovering from the sleep mode, the card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the card is in Idle mode, the card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

5.1.2 Execute Drive Diagnostic – 90h

The Executive Drive Diagnostic command in Table 5.1.2-1 performs the internal diagnostic tests implemented by the card.

Table 5.1.2-1 Executive Drive Diagnostic

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

The Diagnostic codes shown in Table 5.1.2-2 are returned in the Error Register at the end of the command.

Table 5.1.2-2 Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Failed (True IDE Mode)

5.1.3 Erase Sector(s) – C0h

The Erase Sectors command is shown in Table 5.1.3

Table 5.1.3 Erase Sectors

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

The sectors indicated in the task file are left in erased states. Some applications may experience an increase in write performance as a result of this command. Erased sectors return all zero data when read.

5.1.4 Format Track – 50h

The Format Track command in Table 5.1.4 is no longer recommended. This command is supported to guarantee backward compatibility.

Table 5.1.4 Format Track

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive		Head (LBA 27-24)		
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	X (LBA 7-0)							
See Cnt (1)	Count (LBA mode only)							
Feature (1)	X							

This command writes the desired head and cylinder of the selected drive with an FFh pattern. To remain host backward compatible, the card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256).

5.1.5 Identify Drive – ECh

The Identify Drive command in Table 5.1.5-1 enables the host to receive parameter information from the card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5.1.5-2 All reserved bits or words are zero. Table 5.1.5-2 is the definition for each field in the Identify Drive Information.

NOTES: PC Card response differs from CompactFlash.
I-TEMP products report different timing mode support than C-TEMP products.

Table 5.1.5-1 Identify Drive

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

Table 5.1.5-2 Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah(1)	2	General configuration bit-significant information.
1	XXXX	2	Default number of cylinders.
2	0000h	2	Reserved.
3	XXXX	2	Default number of heads.
4	0000h	2	Number of unformatted bytes per track.
5	0240h	2	Number of unformatted bytes per sector.
6	XXXX	2	Default number of sectors per track.
7-8	XXXX	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW).
9	0000h	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0002h	2	Buffer type (dual ported).
21	0002h	2	Buffer size in 512 byte increments.
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands.
23-26	aaaa	8	Firmware revision in ASCII (Rev M.ms) set by code Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	0001h	2	Maximum of 1 sector on Read/Write Multiple command.
48	0000h	2	Double Word not supported.
49	0300h(2)	2	Capabilities: DMA Supported (bit 8), LBA supported (bit 9).
50	0000h	2	Reserved.
51	0203h	2	PIO data transfer cycle timing mode.
52	0000h	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0003	2	Field validity.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	010Xh	2	Multiple sector setting is valid.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000h	2	Single Word DMA Transfer (not supported).
63	0404h(2)	2	0-7: Multiword DMA modes supported. 15-8: Multiword DMA mode active.
64	0003h	2	Advanced PIO modes supported.
65	0078h(2)	2	Minimum Multiword DMA Transfer cycle time per word in ns.
66	0078h(2)	2	Recommended Multiword DMA Transfer cycle time per word in ns.
67	0078h	2	Minimum PIO transfer without flow control.
68	0078h	2	Minimum PIO transfer with IORDY flow control.
69-127	0000h	130	Reserved.
128-159	0000h	64	Reserved vendor unique bytes.
160-255	0000h	192	Reserved.

1. CompactFlash and PCMCIA cards in True IDE mode report 044AH.
2. Multiword DMA is supported. For all unsupported cases, 0100H is reported in word 49, and 0000H is reported in words 52, 63, and 65. CompactFlash products will support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

5.1.5.1 Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10-Mb/sec and is not MFM encoded. CompactFlash products report 848Ah in compliance with the CFA specification. In True IDE mode, the product reports 044Ah indicating the drive is not removable.

5.1.5.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

5.1.5.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

5.1.5.4 Word 4: Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

5.1.5.5 Word 5: Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

5.1.5.6 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

5.1.5.7 Word 7-8: Number of Sectors per Card

This field contains the number of sectors of the product. This double word value is also the first invalid address in LBA translation mode.

5.1.5.8 Word 10-19: Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20h).

5.1.5.9 Word 20: Buffer Type

This field defines the buffer capability with the 0002h meaning a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the card.

5.1.5.10 Word 21: Buffer Size

This field defines the buffer capacity of 2 sectors or 1 kilobyte of SRAM.

5.1.5.11 Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

5.1.5.12 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

5.1.5.13 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

5.1.5.14 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

5.1.5.15 Word 48: Double Word Support

This field indicates this product will not support double word transfers.

5.1.5.16 Word 49: Capabilities

This field indicates if this product supports DMA Data transfers and LBA mode. All TRS* Tele-Radio-Space GmbH products support LBA mode. Multiword DMA operation is supported by PCMCIA products in IDE mode. After CF Specification, Rev 2.1 releases, CompactFlash cards will be available with multiword DMA functionality.

5.1.5.17 Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for Standard and Extended Temperature products fall into categories that have different parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in In Table 3.3.12.2-2, t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements are greater than the sum of t2 and t2i. This means a host implementation may lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

The *IORD-data tri-state* parameter specifies the time from the negation edge of /IORD to the time that the data bus is no longer driven by the device (tri-state).

Table 3.3.12.2-1 with the contents of this field.

NOTE: For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode it can support (i.e., PIO mode 0, 1 or 2).

5.1.5.18 Word 52: Single Word DMA Data Transfer Cycle Timing Mode

This field states this product doesn't support Single Word DMA data transfer mode.

5.1.5.19 Word 53: Translation Parameter Valid

Bit 0 of this field is set, indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. Bit 1 is also set, indicating values in words 64 through 70 are valid.

5.1.5.20 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

5.1.5.21 Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

5.1.5.22 Word 59: Multiple Sector Setting

This field contains a validity flag in the odd byte, and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01H, which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00H, which indicates that R/W Multiple commands are not valid. The only other value returned by the card in the even byte is a 01h value, which indicates that 1 sector per interrupt, can be transferred in R/W Multiple mode.

5.1.5.23 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the card in LBA mode only.

5.1.5.24 Word 64: Advanced PIO Transfer Modes Supported

In Standard Temperature products, bits 0 and 1 of this field are set to indicate support for PIO transfer modes 3 and 4, respectively.

5.1.5.25 Word 65: Minimum Multiword DMA Transfer Cycle Time per Word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

CompactFlash products support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

5.1.5.26 Word 66: Recommended Multiword DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under minimal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less that this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance *may* result.

CompactFlash products support multiword DMA in anticipation of the CF Specification Rev. 2.1 release.

5.1.5.27 Word 67: Minimum PIO Transfer Cycle Time without Flow Control

This field indicates in nanoseconds, the minimum cycle time that, if used by the host, the card guarantees data integrity during the cycle without utilization of flow control.

5.1.5.28 Word 68: Minimum PIO Transfer Cycle Time with Flow Control

This field indicates in nanoseconds, the minimum cycle time the card supports while performing data transfers using flow control.

5.1.6 Idle – 97h, E3h

The Idle command in Table 5.1.6 causes the card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

Table 5.1.6 Idle

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3h or 97h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	Timer Count (5 msec increments)							
Feature (1)	X							

5.1.7 Idle Immediate – 95h, E1h

Table 5.1.7 Idle Immediate

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1h or 95h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.8 Initialize Drive Parameters – 91h

The Initialize Drive Parameters command in Table 5.1.8 causes the card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt. This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

Table 5.1.8 Initialize Drive Parameters

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads -1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	Number of Sectors							
Feature (1)	X							

NOTE: TRS* Tele-Radio-Space GmbH recommends NOT using this command in any system because DOS determines the offset to the Boot Record based on the number of heads and sectors per track. If a card is “Formatted” with one head and sector per track value, the same card will not operate correctly with DOS configured with another heads and sectors per track value.

5.1.9 Read Buffer – E4h

The Read Buffer command in Table 5.1.9 enables the host to read the current contents of the CompactFlash Memory Card’s sector buffer. This command has the same protocol as the Read Sector(s) command.

Table 5.1.9 Read Buffer

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.10 Read DMA Command – C8h, C9h

The Read DMA command in Table 5.1.10 executes in a similar manner to the READ SECTOR(S) command except for the following:

- The host initialises the DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the DMA channel.
- The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read DMA command, the device provides status of the BSY bit or the DRQ bit until the command is completed.

Table 5.1.10. Read DMA

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CBh or C9h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.11 Read Multiple – C4h

The Read Multiple command in Table 5.1.11 performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple, command.

Table 5-.1.11 Read Multiple

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

NOTE: The current revision of the card only supports a block count of 1 as indicated in the Identify Drive Information command. This command is provided for compatibility with future products that may support a larger block count.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = (sector count)—module (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

5.1.12 Read Long Sector – 22h, 23h

The Read Long command in Table 5.1.12 performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of random data transferred in byte mode. Random data is returned instead of ECC bytes because of the nature of the ECC system used. This command has the same protocol as the Read Sector(s) command.

Table 5.1.12 Read Long Sector

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	X							
Feature (1)	X							

5.1.13 Read Sector(s) – 20h, 21h

The Read Sector(s) command in Table 5.1.13 reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Table 5.1.13 Read Sectors

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.14 Read Verify Sector(s) – 40h, 41h

The Read Verify Sector(s) command in Table 5.1.14 is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Memory Card sets BSY.

When the requested sectors have been verified, the card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the “verify” terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 5.1.14 Read Verify Sectors

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.15 Recalibrate – 1Xh

The Recalibrate command in Table 5.1.15 is effectively a NOP command to the card and is provided for compatibility purposes. After this command is executed the Cyl High and Cyl Low as well as the Head number will be 0 and Sec Num will be 1 if LBA=0 and 0 if LBA=1 (i.e., the first block in LBA is 0 while CHS mode the sector number starts at 1).

Table 5.1.15 Recalibrate

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.16 Request Sense – 03h

The Request Sense command in Table 5.1.16-1 requests an extended error code after a command ends with an error.

Table 5.1.16-1 Request Sense

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

Table 5.1.16-2 defines the valid extended error codes for Standard ATA products. The extended error code is returned to the host in the Error Register. This command must be the next command issued to the card following the command that returned an error.

Table 5.1.16-2 Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write/Erase Failed

5.1.17 Seek – 7Xh

The Seek command in Table 5.1.17 is effectively a NOP command to the card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

Table 5.1.17 Seek

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	X (LBA 7-0)							
See Cnt (1)	X							
Feature (1)	X							

5.1.18 Set Features – EFh

The Set Features command in Table 5.1.18-1 is used by the host to establish or select certain features.

Table 5.1.18-1 Seat Features

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	Config							
Feature (1)	Feature							

Table 5.1.18-2 defines all features that are supported. Please note that the 9Ah feature is unique to the CompactFlash Memory Card and are not part of the ATA Specification.

Table 5.1.18-2 Features Supported

Feature	Operation
01h	Enable 8-bit data transfer.
03h	Set Transfer mode based on value in Sector Count register.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	Accepted for backward compatibility with the legacy TRS* Tele-Radio-Space GmbH ATA products but has no impact on the card.
81h	Disable 8-bit data transfer.
96h	Accepted for backward compatibility with the legacy TRS* Tele-Radio-Space GmbH ATA products but has no impact on the card.
9Ah	Accepted for backward compatibility with the legacy TRS* Tele-Radio-Space GmbH ATA products, but has no impact on the card.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer mode. If the 01h feature command is issued, all data transfers will occur on the low order D7-D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 55h and BBh are the default features for the card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature 9Ah is accepted for backward compatibility with legacy TRS* Tele-Radio-Space GmbH ATA products but has no impact on the card. TRS* Tele-Radio-Space GmbH does not recommend the use of this command in new designs.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs. POR defaults the number of heads and sectors along with 16 bit data transfers and the read/write multiple block count.

A host can choose the transfer mechanism by Set Transfer mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value (refer to Table 5.1.18-3).

Table 5.1.18-3 Features Supported

PIO Default Transfer Mode	00000 00d
PIO Flow Control Transfer Mode x	00001 nnn
Multiword DMA Mode x	00100 nnn
Reserved	01000 nnn
Reserved	01000 nnn

NOTE: “nnn” is a valid mode number in binary, “x” is the mode number in decimal for the associated transfer type, and “d” is ignored.

5.1.19 Set Multiple Mode – C6h

The Set Multiple Mode command in Table 5.1.19 enables the card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. The current version of the card supports only a block size of 1 sector per block. Future versions may support larger block sizes. Upon receipt of the command, the product sets BSY to 1 and checks the Sector Count Register.

Table 5.1.19 Seat Multiple Mode

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	Sector Count							
Feature (1)	X							

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

5.1.20 Set Sleep Mode – 99h, E6h

The Set Sleep Mode command in Table 5.1.20 causes the card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the read to sleep timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

Table 5.1.20 Set Sleep Mode

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6h or 99h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.21 Standby – 96h, E2h

The Standby command in Table 5.1.21 causes the card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY, and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Table 5.1.21. Standby

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2h or 96h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.22 Standby Immediate – 94h, E0h

The Standby Immediate command in Table 5.1.22 causes the card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Table 5.1.22 Standby Immediate

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0h or 94h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.23 Translate Sector – 87h

When the Translate Sector command in Table 5.1.23-1 is issued, the controller responds with a 512-byte buffer of information on the desired cylinder, head and sector with the actual Logical Address.

Table 5.1.23-1 Translate Sector

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	X							
Feature (1)	X							

Table 5.1.23-2 represents the information in the buffer. Please note that this command is unique to TRS* Tele-Radio-Space GmbH Standard ATA products.

Table 5.1.23-2 Translate Sector Information

Address	Information
00	Head
01-02	Cylinder
03	Sector
04-07	LBA
08	Chip
09-0A	Block
0B	Page
0c-1FF	Reserved

5.1.24 Wear Level – F5h

The Wear Level command in Table 5.1.24 is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed.

Table 5.1.24 Wear Level

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	Completion Status							
Feature (1)	X							

5.1.25 Write Buffer – E8h

The Write Buffer command in Table 5.1.25 enables the host to overwrite contents of the card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

Table 5.1.25 Write Buffer

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (2)	X							
See Cnt (1)	X							
Feature (1)	X							

5.1.26 Write DMA Command – CAh, CBh

The Write DMA command in Table 5.1.26 executes in a similar manner to WRITE SECTOR(S) except for the following:

- The host initialised the DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the DMA channel.
- The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write DMA command, the device provides status of the BSY bit or the DRQ bit until the command is completed.

Table 5.1.26 Write DMA

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAh or CBh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.27 Write Long Sector – 32h, 33h

The Write Multiple command in Table 5.1.27 is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state card, the four bytes of ECC transferred by the host cannot be used by the card. The card discards these four bytes and writes the sector with valid ECC fields. This command has the same protocol as the Write Sector(s) command.

Table 5.1.27 Write Long Sector

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	X							
Feature (1)	X							

5.1.28 Write Multiple Command – C5h

The Write Multiple command in Table 5.1.28 is similar to the Write Sectors command. The card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

Table 5.1.28 Write Multiple Command

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (2)	Sector Number							
See Cnt (1)	Sector Count							
Feature (1)	X							

NOTE: The current revision of the Standard ATA product only supports a block count of 1 as indicated in the Identify Drive Command information. This command is provided for compatibility with future products that may support a larger block count.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count/block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

5.1.29 Write Multiple without Erase – CDh

TRS* Tele-Radio-Space GmbH does not recommend the use of the Write Multiple without Erase command in new designs but it is supported as a normal Write Sectors command for backward compatibility reasons.

Table 5.1.29 Write Multiple without Erase

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (2)	Sector Number							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.30 Write Sector(s) – 30h, 31h

The Write Sectors command in Table 5.1.30 writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

Table 5.1.30 Write Sectors

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.
If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

5.1.31 Write Sector(s) without Erase – 38h

TRS* Tele-Radio-Space GmbH does not recommend the use of this command in new designs but it is supported as a normal Write Sectors command for backward compatibility reasons.

Table 5.1.31 Write Sectors without Erase

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

5.1.32 Write Verify Sector(s) – 3Ch

The Write Verify Sector(s) command in Table 5.1.32 writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. No data should be transferred by the host until BSY has been cleared by the host.

Table 5.1.32 Writer Verify Sectors

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (2)	Sector Number (LBA 7-0)							
See Cnt (1)	Sector Count							
Feature (1)	X							

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

5.2 Error Posting

Table 5.2 summarizes the valid status and error value for all the ATA Command set.

Table 5.2 Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic(1)						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read DMA(2)	V	V	V	V	V	V	V	V	V	V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write DMA(2)	V		V	V		V	V			V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify Sector(s)	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

V = valid on this command.

1. See Table 5.1.1
2. CompactFlash products support multiword DMA in anticipation of the CF Specification Rev. 2.1 release. PCMCIA products support multiword DMA operation in True IDE mode only.

6. CIS (Card Information Structure) Description

This section describes the Card Information Structure (CIS) for the TRS Star CompactFlash Memory Cards.

Table 6. Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	03h	TPL_LINK								Link is 3 bytes	Link to next Tuple
004h	D9	Dev ID Type Dh=I/O				W 1	Speed 1h=250ns			I/O Device, No WPS, speed=250ns if no wait	Device ID, WPS, Speed
006h	01h	#address unit-1= 1 unit					Size Code = 2K units			(One) 2 Kilobytes of address space	Device Size
008h	FFh	CISTPL_END								End of CISTPL_DEVICE	End Marker
00Ah	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Ch	04h	TPL_LINK								Link is 4 bytes	Link to next tuple
00Eh	02h	Reserved 0						3 0	W 1	Conditions: 3V operation is allowed, and WAIT is used	3 Volts Operation, Wait Function
010h	D9h	Dev ID Type Dh=I/O				W 1	Speed 1h=250ns			I/O Device, No WPS, speed = 250 ns if no wait	Device ID, WPS, Speed
012h	01h	#address unit-1 = 1 unit				Size Code = 2K units				(One) 2 Kilobytes of address space	Device Size
014h	FFh	CISTPL_END								End of CISTPL_DEVICE	End Marker
016h	18h	CISTPL_JEDEC_C								JEDEC programming info Tulpe	Tuple Code
018h	02h	TPL_LINK								Link is 2 bytes	Link Length
01Ah	DFh	JEDEC ID								Device Manufactor ID	Manufactor ID
01Ch	01h	JEDEC Info								Manufacturer specific info	Manufacturer info
01Eh	20h	CISTPL_MANFID								Manufacturer ID tuple	Tuple code
020h	04h	TPL_LINK								Link length is 4 bytes	Link to next tuple
022h	00h	TPLMID_MANF								PC Card manufacturer code	Manufacturer ID
024h	00h										
026h	00h	TPLMID_CARD								Manufacturer specific info	Manufacturer info
028h	00h										
02Ah	21h	CISTPL_FUNCID								Function ID tuple	Tuple code
02Ch	02h	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
02Eh	04h	TPLFID_FUNCTION								Fixed disk drive	Function code
030h	01h	Reserved						R	P	R=0: no expansion ROM P=1: configure at POST	System init byte TPLFID_SYSINIT
032h	22h	CISTPL_FUNCE								Function Extension tuple	Tuple code
034h	02h	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
036h	01h	Disk function extension tuple								Disk interface information	TPLFE_TYPE
038h	01h	Disk interface type								PC card ATA interface	TPLFE_DATA
03Ah	22h	CISTPL_FUNCE								Function Extension tuple	Tuple code
03Ch	03h	CISTPL_LINK								Link length is 3 bytes	Link to next tuple
03Eh	02h	Disk function extension tuple								PC card ATA basic features	TPLFE_TYPE

TRS Star Specification

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
040h	04h	Reserved				D	U	S	V	D=0:single drive on card U=0: no unique serial number S=1: silicon device V=0: no VPP required	TPLFE_TYPE
042h	07h	R	I	E	N	P				I=0: twin IOIS16# unspecified E=0: index bit not emulated N=0: I/O includes 0x3F7 P=7: sleep, standby, idle supported	TPLFE_TYPE
044h	1Ah	CISTPL_CONFIG								Configuration Tuple	Tuple code
046h	05h	TPL_LINK								Link length is 5 bytes	Link to next tuple
048h	01h	RFS		RMS				RAS		RFS: reserved RMS: 1 byte register mask RAS: 2 bytes base address	Size of fields TPCC_SZ
04Ah	07h	TPCC_LAST								Last configuration entry is 07H	Last entry index
04Ch	00h	TPCC_RADR (LSB)								Configuration registers are located at 0200h	Configuration register location
04Eh	02h	TPCC_RADR (MSB)									
050h	0Fh	TPCC_RMSK								Configuration registers 0 to 3 are present	Configuration register present mask
052h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
054h	0Bh	CISTPL_LINK								Link length is 11 bytes	Link to next tuple
056	C0h	I	D	Configurations Index						Memory mapped configuration, index=0 I=1: Interface byte follows D=1: Default entry	Configuration Table Index Byte TPCE_INDX
058h	C0h	W	R	P	B	Interface Type				W=1: wait required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=0: Memory interface	Interface Description TPCE_IF
05Ah	A1h	M	MS		IR	IO	T	Power		M=1: misc info present MS=1: 2 byte memory length IR=0: no interrupt is used IO=0: no I/O space is used T=0: no timing info specified Power=1: VCC info, no VPP	Feature Selection Byte TPCE_FS
05Ch	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	Power Description Structure Parameter Selection Byte TPCE_PD
05Eh	55h	X	Mantisse			Exponent				Nominal voltage 5.0V	
060h	4Dh	X	Mantisse			Exponent				Minimum voltage 4.5V	
062h	5Dh	X	Mantisse			Exponent				Maximum voltage 5.5V	
064h	75h	X	Mantisse			Exponent				Peak current 80 mA	
066h	08h	Length in 256 byte units (LSB)								Length of memory space is 2 KByte	Memory space descr. TPCE_MS
068h	00H	Length in 256 byte units (MSB)									
06Ah	21h	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	Miscellaneous features TPCE_MI
06Ch	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code

TRS Star Specification

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
06Eh	06h	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
070h	00h	I	D	Configurations Index						Memory mapped configuration, index=0	TPCE_INDX
072h	01h	M	MS		IR	IO	T	Power		Power=1: VCC info, no VPP	TPCE_FS
074h	21h	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
076h	B5h	X	Mantisse			Exponent				X=1: extension byte present	
078h	1Eh	X	Extension							Nominal voltage 3.30V	
07Ah	4Dh	X	Mantisse			Exponent				Peak current 45 mA	
07Ch	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
07Eh	0Dh	CISTPL_LINK								Link length is 13 bytes	Link to next tuple
080h	C1h	I	D	Configuration Index						I/O mapped, index=1 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
082h	41h	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
084h	99h	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: VCC info, no VPP	TPCE_FS
086h	27h	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
088h	55h	X	Mantisse			Exponent				Nominal voltage 5.0V	
08Ah	4Dh	X	Mantisse			Exponent				Minimum voltage 4.5V	
08Ch	5Dh	X	Mantisse			Exponent				Maximum voltage 5.5V	
08Eh	75h	X	Mantisse			Exponent				Peak current 80 mA	
090h	64h	R	S	E	IO					S=1: support 16 bit hosts E=1: support 8 bit hosts IO=4: 4 address lines decoded	TPCE_IO
092h	F0h	S	P	L	M	V	B	I	N	S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=1: masks V..N present V=0: no vendor unique IRQ B=0: no bus error IRQ I=0: no I/O check IRQ N=0: no NMI	TPCE_IR
094h	FFh	IRQ7..0								Interrupt signal may be assigned to any host IRQ	
096h	FFh	IRQ15..8									
098h	21h	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
09Ah	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
09Ch	06h	CISTPL_LINK								Link length is 6 bytes	Link to next tuple

TRS Star Specification

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
09Eh	01h	I	D	Configuration index						I/O mapped, index=1	TPCE_INDX
0A0h	01h	M	MS		IR	IO	T	Power		Power=1: VCC info, no VPP	TPCE_FS
0A2h	21h	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0A4h	B5h	X	Mantisse			Exponent				X=1: extension byte present	
0A6h	1Eh	X	Extension							Nominal voltage 3.30V	
0A8h	4Dh	X	Mantisse			Exponent				Peak current 45 mA	
0AAh	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0ACh	12h	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0AEh	C2h	I	D	Configuration Index						I/O mapped, index=2 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0B0h	41h	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0B2h	99h	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: VCC info, no VPP	TPCE_FS
0B4h	27h	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0B6h	55h	X	Mantisse			Exponent				Nominal voltage 5.0V	
0B8h	4Dh	X	Mantisse			Exponent				Minimum voltage 4.5V	
0Bah	5Dh	X	Mantisse			Exponent				Maximum voltage 5.5V	
0BCh	75h	X	Mantisse			Exponent				Peak current 80 mA	
0Beh	EAh	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0C0h	61h	LS		AS		NR				LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0C2h	F0h	Base address 1 (LSB)								Address range 1 0x1F0 to 0x1F7	
0C4h	01h	Base address 1 (MSB)									
0C6h	07h	Address range 1 length									
0C8h	F6h	Base address 2 (LSB)								Address range 2 0x3F6 to 0x3F7	
0CAh	03h	Base address 2 (MSB)									
0CCh	01h	Address range 2 length									
0CEh	EEh	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR

TRS Star Specification

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
0D0h	21h	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
0D2h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0D4h	06h	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
0D6h	02h	I	D	Configuration Index						I/O mapped, index=2	TPCE_INDX
0D8h	01h	M	MS		IR	IO	T	Power		Power=1: VCC info, no VPP	TPCE_FS
0DAh	21h	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0DCh	B5h	X	Mantisse			Exponent				X=1: extension byte present	
0DEh	1Eh	X	Extension							Nominal voltage 3.30V	
0E0h	4Dh	X	Mantisse			Exponent				Peak current 45 mA	
0E2h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0E4h	12h	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0E6h	C3h	I	D	Configuration Index						I/O mapped, index=3 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0E8h	41h	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0EAh	99h	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: VCC info, no VPP	TPCE_FS
0ECh	27h	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0EEh	55h	X	Mantisse			Exponent				Nominal voltage 5.0V	
0F0h	4Dh	X	Mantisse			Exponent				Minimum voltage 4.5V	
0F2h	5Dh	X	Mantisse			Exponent				Maximum voltage 5.5V	
0F4h	75h	X	Mantisse			Exponent				Peak current 80 mA	
0F6h	EAh	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0F8h	61h	LS		AS		NR				LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0FAh	70h	Base address 1 (LSB)								Address range 1 0x170 to 0x177	
0FCh	01h	Base address 1 (MSB)									
0FEh	07h	Address range 1 length									
100h	76h	Base address 2 (LSB)								Address range 2 0x376 to 0x377	
102h	03h	Base address 2 (MSB)									
104h	01h	Address range 2 length									

TRS Star Specification

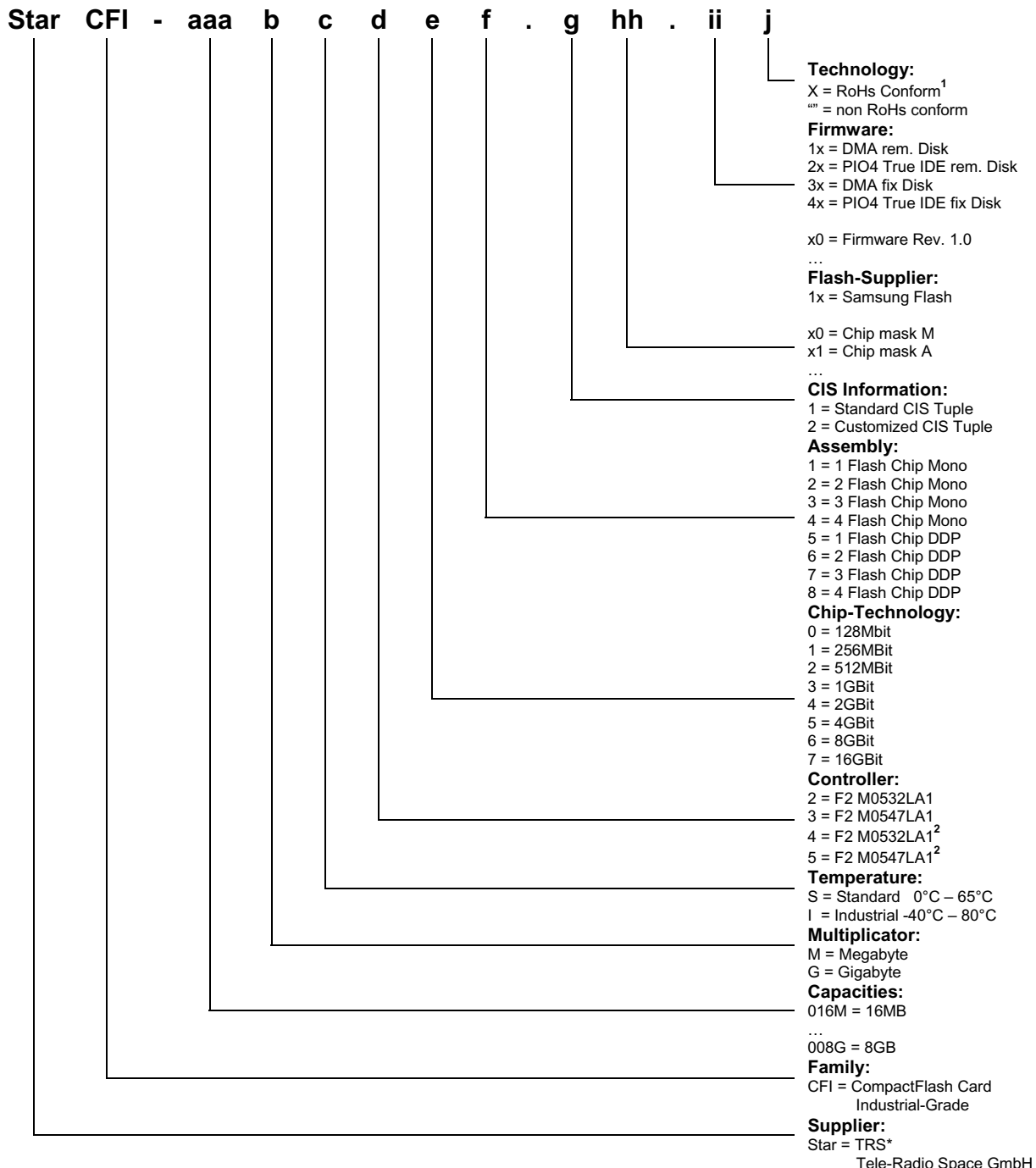
Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
106h	EEh	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
108h	21h	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
10Ah	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
10Ch	06h	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
10Eh	03h	I	D	Configuration Index						I/O mapped, index=3	TPCE_INDX
110h	01h	M	MS		IR	IO	T	Power		Power=1: VCC info, no VPP	TPCE_FS
112h	21h	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
114h	B5h	X	Mantisse			Exponent				X=1: extension byte present	
116h	1Eh	X	Extension							Nominal voltage 3.30V	
118h	4Dh	X	Mantisse			Exponent				Peak current 45 mA	
11Ah	1Bh	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
11Ch	04h	CISTPL_LINK								Link length is 4 bytes	Link to next tuple
11Eh	07h	I	D	Configuration Index						I/O mapped, index=7	TPCE_INDX
120h	00h	M	MS		IR	IO	T	Power		No feature descriptions follow	TPCE_FS
122h	28h									TRS Star specific data	
124h	D3h									TRS Star specific data	
126h	14h	CISTPL_NO_LINK								No link control tuple	Tuple code
128h	00h	CISTPL_LINK								Link length is 0 bytes	Link to next tuple
12Ah	15h	CISTPL_VERS_1								Level 1 version/product info	Tuple code
12Ch	15h	CISTPL_LINK								Link length is 21 bytes	Link to next tuple
12Eh	04h	TPPLV1_MAJOR								PCMCIA2.0/JEIDA4.1	Major version
130h	01h	TPPLV1_MINOR								PCMCIA2.0/JEIDA4.1	Minor version
132h	54h									“T”	Info String 1 (TRS* Star)
134h	52h									“R”	
136h	53h									“S”	
138h	2Ah									“*”	
13Ah	20h									“ “	
13Ch	53h									“S”	
13Eh	74h									“t”	
140h	61h									“a”	
142h	72h									“r”	
144h	00h									Null	End of String 1
146h	53h									“S”	Info String 2 Article No: Example: Star CFI-512MS242.110.10
148h	74h									“t”	
14Ah	61h									“a”	

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
14Ch	72h									“r”	
14Eh	20h									“ ”	
150h	43h									“C”	
154h	46h									“F”	
156h	49h									“I”	
158h	2Dh									“-”	
15Ah	35h									“5”	
15Ch	31h									“1”	
15Eh	32h									“2”	
160h	4Dh									“M”	
162h	53h									“S”	
164h	32h									“2”	
166h	34h									“4”	
168h	32h									“2”	
16Ah	2Eh									“.”	
16Ch	31h									“1”	
16Eh	31h									“1”	
170h	30h									“0”	
172h	2Eh									“.”	
174h	31h									“1”	
176h	30h									“0”	
178h	00h									Null	End of String 2
17Ah	31h									“1”	Info String 3 Ordering No and Serial No into this lot: Example: 10203205360 00000000
17Ch	30h									“0”	
17Eh	32h									“2”	
180h	30h									“0”	
182h	33h									“3”	
184h	32h									“2”	
186h	30h									“0”	
188h	35h									“5”	
18Ah	33h									“3”	
18Ch	36h									“6”	
18Eh	30h									“0”	
18Ch	20h									“”	
190h	30h									“0”	
192h	30h									“0”	
194h	30h									“0”	
196h	30h									“0”	
198h	30h									“0”	

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	Cis Funktion
19Ah	30h									"0"	
19Ch	30h									"0"	
19Eh	30h									"0"	
1A0h	00h									Null	End of String 3
1A2h	FFh	CISTPL_END								End of CISTPL_VERS_1	End marker
1A4h	FFh	CISTPL_END								End of CIS	Tuple code

7. Ordering Information Industrial-Grade

Table 7. Ordering Information



Note: [1] available in Q1/2006
[2] only for realtime application with Firmware Rev. x3

8. TRS* Star Back-Side Label Specification

Figure 8. Backside Label TRS* Star Industrial-Grade CompactFlash Cards

Table 8. Back-Side Label Specification

.	Type	Description
1	Logo TRS*	TRS* Tele-Radio-Space GmbH Industriestrasse 5 76297 Stutensee Germany http://www.trs-star.com
2	Article – No:	Please, refer the "Ordering Information" under section 7 for more information
3	Barcode	Barcode Information based on the Code EAN128C 8 characters
4	TÜV-SÜD	NRTL certification for the UL60950-1, UL60950-21, CSA C22.2
5	RoHS	The TRS approval for the European Directive 2002/96/EC RoHS (Restriction of Hazardous Substances)
6	CE	Please, refer the "EU Declaration of Conformity" under section 12 and the "CE Report" under section 13
7	CF	TRS* Tele-Radio-Space GmbH is a member of CFA. The CF- Card is compatible to the CF-Spec. 2.0 Link: http://www.compactflash.org
8	Lot – No:	Production Lot-No
9	WEEE	The approval for the European Directive 2002/96/EC WEEE (Waste Electrical and Electronical Equipment) WEEE-Reg.-Nr.DE75459432

9. Technical Support Services Worldwide Web Site

Internet users can obtain technical support and product information along with news and much more from the TRS* Tele-Radio-Space GmbH Worldwide Web Site, 24 hours a day, seven days a week. The TRS* Tele-Radio-Space GmbH Worldwide Web Site is frequently updated.
Visit this site often to obtain the most up-to-date information on TRS* Tele-Radio-Space GmbH products.

The TRS* Tele-Radio-Space GmbH have following Web Site. The URLs are:

Technical Suite for Industrial-Grade, Standard-Grade and Digital-Grade CompactFlash Cards:

http://www.trs-star.com.
http://www.trs-star.de.

Internet-Shop for Flash Cards, USB-Sticks, USB-Harddisks, USB-Musicsticks, Memory-Modules and more::

http://www.trs-space.com.

10. Sales Offices

For TRS* Star Industrial-Grade and Standard-Grade CompactFlash Cards:

TRS* Tele-Radio-Space GmbH
Headquarters
Attn: IS-Grade
Industriestrasse 5
D-76297 Stutensee
Germany

Tel.: +49(0)7249/910340
Fax: +49(0)7249/910350
Email: us@trs-star.com
WEB: http://www.trs-star.com

For other TRS* Tele-Radio-Space GmbH products use:

TRS* Tele-Radio-Space GmbH
Headquarters
Attn: Internet
Industriestrasse 5
D-76297 Stutensee
Germany

Tel.: +49(0)7249/910386
Fax: +49(0)7249/910387
Email: info@trs-space.de
WEB: http://www.trs-space.de

To order Online in our Internetshop use the World Wide Web Suite: http://www.trs-space.de,
or sent your inquery via email to following emailadresses:

info@trs-star.com
info@trs-space.de.

11. Receiving Warranty Service

According to TRS* Tele-Radio-Space GmbH warranty procedure, defective product should be returned only with prior authorization from TRS* Tele-Radio-Space GmbH. Please contact download the RMA-formsheet from the worldwide Web Suite http://www.trs-star.com and sent it via mail to rma@trs-star.com or Fax: +49(0)7249/910387 with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, TRS* Tele-Radio-Space GmbH will issue a **R**eturn **M**aterial **A**uthorization (RMA) or **P**roduct **R**epair **A**uthorization (PRA) number. Ship the defective product to:

TRS* Tele-Radio-Space GmbH
Headquarters
Attn: RMA TRS-Star
Industriestrasse 5
D-76297 Stutensee
Germany

12. EU Declaration of Conformity

No. 1.05105.01.TRS, dated 10.05.2005

Manufacturer: **TRS* Tele-Radio-Space GmbH**
Industriestrasse 5
D-76297 Stutensee
Germany

Product Description:

TRS Star Industrial-Grade CompactFlash™ Cards

Product Family:

STAR CFI-016Mxyyy.zzz.aa, STAR CFI-032Mxyyy.zzz.aa, STAR CFI-048Mxyyy.zzz.aa,
STAR CFI-064Mxyyy.zzz.aa, STAR CFI-096Mxyyy.zzz.aa, STAR CFI-128Mxyyy.zzz.aa,
STAR CFI-192Mxyyy.zzz.aa, STAR CFI-256Mxyyy.zzz.aa, STAR CFI-384Mxyyy.zzz.aa,
STAR CFI-512Mxyyy.zzz.aa, STAR CFI-768Mxyyy.zzz.aa, STAR CFI-001Gxyyy.zzz.aa,
STAR CFI-01G5xyyy.zzz.aa, STAR CFI-002Gxyyy.zzz.aa, STAR CFI-004Gxyyy.zzz.aa,
STAR CFI-006Gxyyy.zzz.aa, STAR CFI-008Gxyyy.zzz.aa

We hereby confirm that the family of products named above corresponds with requirements, which have been established in the councils guidelines for the alignment of member states legal provisions with respect to electromagnetic compatibility.
The following standards were referred to in order to assess the product with respect to electromagnetic compatibility and mechanical compatibility:

EG-RL89/336/EWG	Product standard	EN 55022 (Edition 1999)
i.d.F. 93/68/EWG	Basic technical standard	EN 55024 (Edition 1999)
International Standards	CFA CompactFlash™ Association	(Specification 1.1)

Other details regarding the observance of these standards are contained in the TRS* Tele-Radio-Space GmbH master project files and ACCESS-Database.

TRS* Tele-Radio-Space GmbH
Stutensee, 10.05.2005

ppa. Guido Ries
Representative

ppa. Guido Ries
Signature

This declaration certifies the conformity with the guidelines mentioned above, for cases in which these units are part of CE-conforming devices. However, it is not an assurance of characteristics along the lines of Product Liability Law.
The safety instructions belonging to the product documentation supplied should be observed.

13. CE Report

INGENIEURBÜRO DROTLEFF VDI
EMV-Messtechnik - EMV-Labor - EMV-Mobildienst

Elektromagnetische Verträglichkeit EMV

Prüfbericht Nr.: **3041C81**

Auftraggeber: TRS* Tele-Radio-Space GmbH

Prüfgegenstand

Produktname: **Compact Flash Card Type 1**
Produktbezeichnung: **TRS STAR Industrial-Grade**

Ausgabe: 2003
Seriennummer: ---

Hersteller: TRS* Tele-Radio-Space GmbH

Prüfdatum: 16.01.2003

Prüfort: Ing. Büro DROTLEFF VDI
EMV-Labor
Am Heegwald 6, 76227 Karlsruhe

Bericht erstellt von:
Ing. Büro DROTLEFF

Geprüft:

Datum: 24.01.2003

INGENIEURBÜRO DROTLEFF
EMV-Meßtechnik / EMV-Mobildienst
Dipl.Ing. (FH) Klaus Drotleff VDI
Am Heegwald 6 76227 Karlsruhe
Tel.: (0721) 94478-0 Fax: -90
Funktelefon: 0172-7227038

Dieser Bericht besteht aus 14 Seiten

INGENIEURBÜRO DROTLEFF VDI | Dipl. Ing. (FH) Klaus Drotleff | Am Heegwald 6, 76227 Karlsruhe | Fon 0721-94478-0, Fax 0721-94478-90

Inhaltsverzeichnis

1. Angaben zur Prüfung

Auftraggeber

Fa. TRS Tele-Radio-Space GmbH
Industriestraße 5
76297 Stutensee

Herr Guido Ries

Prüfort	EMV-Labor Ingenieurbüro Drotleff VDI Am Heegwald 6, 76227 Karlsruhe
Prüfer	Dipl.-Ing.(FH) Klaus Drotleff
Prüftag/-zeitraum	16.01.2003

Grund der Prüfung: Neues Produkt; CE-Kennzeichnung.

Art der Prüfung Konformitätsprüfung nach EG-RL 89/336/EWG i.d.F. 93/68/EWG

Prüfgrundlagen Auftragsgemäß wurde ausgeführt:

Messung der Störaussendung:
- ☐ Störspannung
- ☒ Störfeldstärke
- ☐ Stromoberschwingungen
- ☐ Flicker

Test der Störfestigkeit:

☐ BURST	☐ geleitete HF
☐ ESD	☐ Spannungseinbrüche/-unterbrüche
☐ Surge	☐ Magnetfelder
☐ gestrahlte HF	☐ sonst

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 3

Angaben zur Prüfung

Normen

Zur Überprüfung der EMV des Prüflings wurden im wesentlichen folgende Normen herangezogen:

- DIN EN 55022:1999	Grenzwerte und Meßverfahren für Funkstörungen von Einrichtungen der Informationstechnik
- DIN EN 55024:1999	Einrichtungen der Informationstechnik - Störfestigkeitseigenschaften

Vervielfältigung und Weitergabe

Dieser Bericht bezieht sich ausschließlich auf die für die Prüfung zur Verfügung gestellten Geräte. Vervielfältigung und Weitergabe nur im vollen Umfang.

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 4

2. PRÜFERGEBNISSE

TEST SPEZIFIKATIONEN UND PRÜFERGEBNISSE
EN 55022 + EN 55024

Test No.	STÖRAUSSENDUNG	Ergebnis	Bemerkungen
1	**STÖRSPANNUNG / Netz** EN 61000-6-3:2001 EN 55022:1998	N/A	
2	**Störfeldstärke** EN 61000-6-3:2001 EN 55022:1998	P	Klasse B
3	Oberschwingungsströme	N/A	
4	Spannungsschwankungen und Flicker	N/A	

Test No.	STÖRFESTIGKEIT	Ergebnis	Bemerkungen
5	ESD - Elektrostatische Entladung -	ND	
6	Hochfrequente Störfelder -HF-	ND	
7	BURST - schnelle transiente Störgrößen	N/A	
8	SURGE - Stoßspannungen -	N/A	
9	Spannungseinbrüche	N/A	
10	Leitungsgeführte HF	N/A	
11	**Magnetfelder**, energietechnische Frequenzen	ND	

P=Passed F=Failed ND=Not Done N/A=Not Applicable

Prüfergebnis:

Die Anforderungen nach EN 55022 werden eingehalten.

3. Angaben zum Prüfobjekt

Hersteller: TRS* Tele-Radio-Space GmbH
Industriestraße 5
76297 Stutensee

Bezeichnung: Compact Flash Card Type 1

Type: TRS STAR Industrial-Grade

Ausgabe: 2003

Beschreibung: ---

Betriebsarten beim Testen:
- Standby: Karte gesteckt.
- Write mode: Karte wird beschrieben.
- Read mode: Karte wird ausgelesen.

Support-Equipment: Der Meßaufbau bestand aus:
- einem Notebook, Marke HP Omnibook xt1000, S/N. TW21308596
- einem Kartenlesegerät, Marke Sitecom Multi Memory Reader Writer, Typ CN-300, S/N. 00035038 mit ca. 1,2m fest angeschlossenem USB-Kabel.
- Windows XP Oberfläche; Beschreiben und Auslesen der Karte mit großen Datenmengen.

Einsatzort: Wohnbereich

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 6

PRÜFOBJEKT

Compact Flash Card: Beispielsweise 512 MByte TRS STAR-CFI-512MS34.000

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 7

4. Störfeldstärke

Normenbezug:

Grenzwerte entsprechend Fachgrundnorm:	EN 61000-6-3:2001
Grundnorm:	EN 55 022 Klasse B
Frequenzbereich:	30 MHz - 1000 MHz
Prüfpunkt/Schnittstelle:	Gehäuse, Kabel
Messentfernung:	1 m

Verwendete Messgeräte:

☒	**EMV Spektrumanalysator** 9 kHz - 1,8 GHz	Hewlett Packard	HP 8591 EM
☒	**HF Verstärker** (25 dB) 9 kHz - 1,3 GHz	Hewlett Packard	HP 8447 F
☐	**Antenne** bikonisch 30 - 300 MHz	EMCO	93110B
☒	**Antenne** log.- per. 200 - 1000 MHz	EMCO	93146
☒	**Antenne** aktive E-Feld Sonde 30 MHz - 1 GHz	Hameg	HZ 530-E4
☐	HF-Dämpfungsglieder 10 dB	MTS	DGL-51010
☐	HF-Dämpfungsglieder 20 dB	MTS	DGL-52010
☐	**Induktive Nahfeldsonde**	KNS	MWB

Messplatz/Messort: Absorberkabine

Modifikationen: keine

Entstörmittel: keine

Bemerkungen: ---

ERGEBNIS: **Der Grenzwert der Klasse B wird eingehalten.**

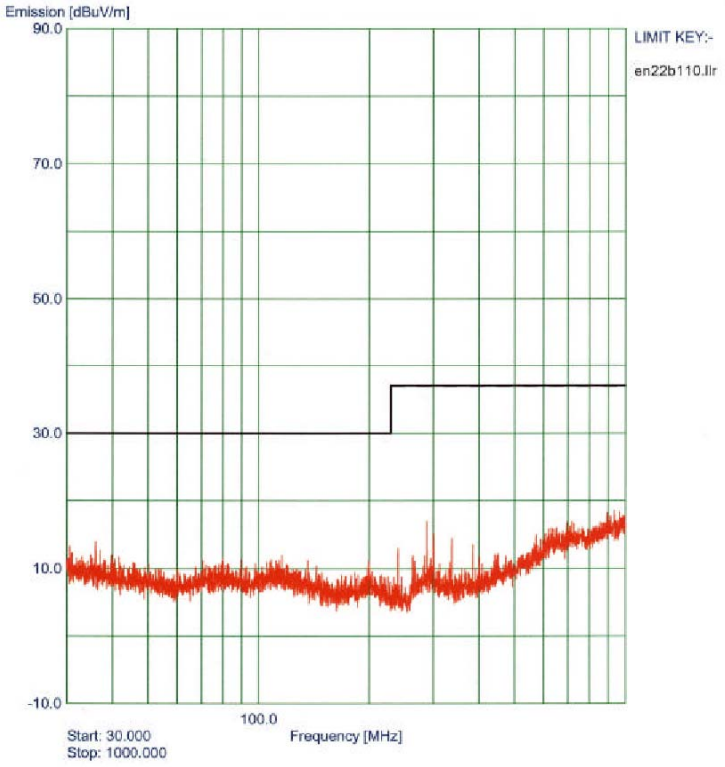
Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 8

Störfeldstärke

Störfeldstärke - Referenz; ohne CF-Card

Filename : c:\emtest\data\msc\cf_cards\ref_1.dat
Oper : Drotleff
Spec : EN 55022, Class B
Type : Radiated Polarisation : Vertical

Comments :
Mit Originalkabel
mit xt1000, USB hinten



RBW: 120.00 kHz
VBW: 300.00 kHz
Device : CF-Reader
Serial #: 00035038
Batch : SITECOM MM CN-300

17:15:29 16 Jan 2003

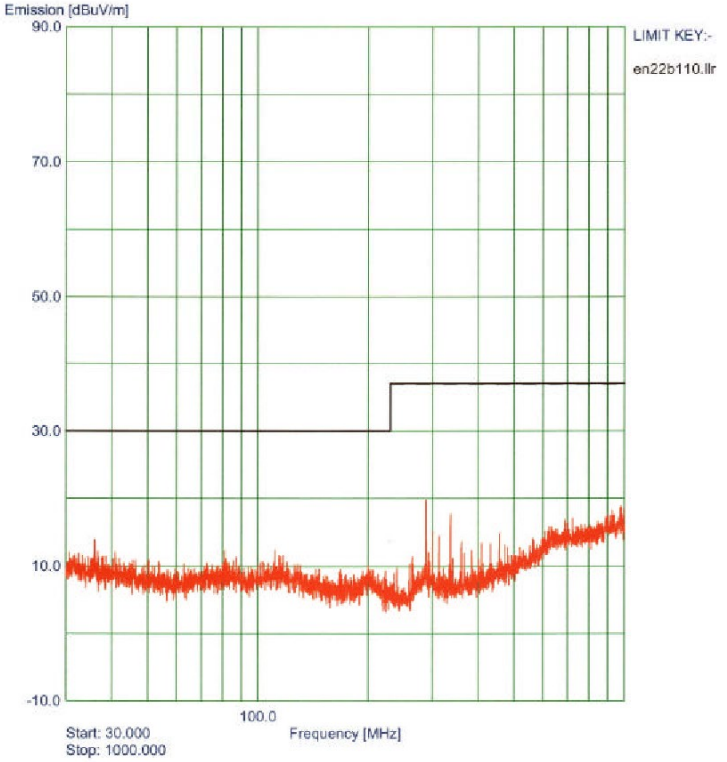
Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 9

Störfeldstärke

Störfeldstärke - standby -

Filename : c:\emtest\data\msc\cf_cards\512_1.dat
Oper : Drotleff
Spec : EN 55022, Class B
Type : Radiated Polarisation : Vertical

Comments :
SITECOM MM CN-300, ref_1
Karte gesteckt



RBW: 120.00 kHz
VBW: 300.00 kHz
Device : CF-Card
Serial #:
Batch : CF-512MS00

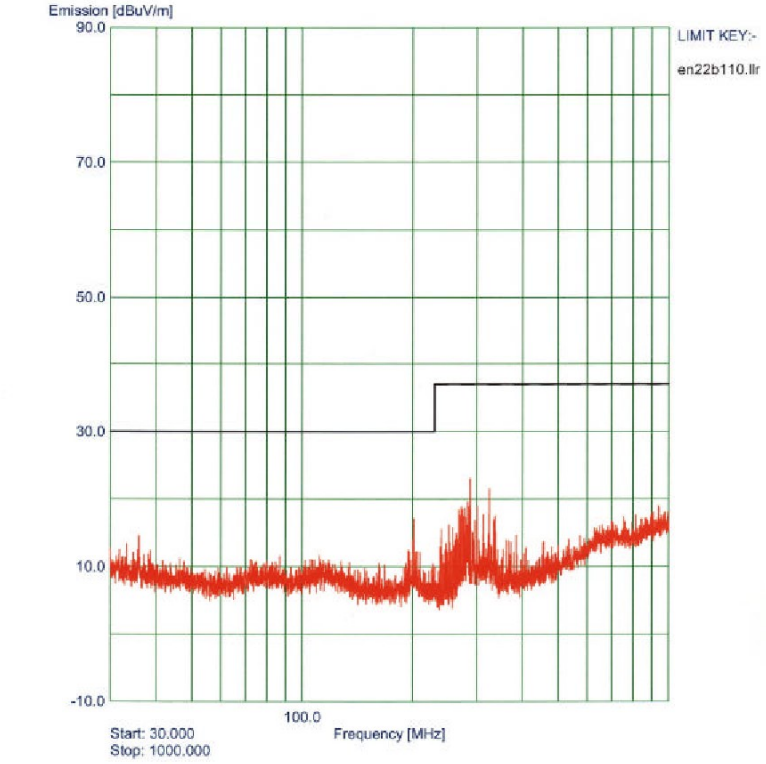
23:11:41 16 Jan 2003

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 10

Störfeldstärke - write mode -

Filename : c:\emtest\data\msc\cf_cards\512_3.dat
Oper : Drotleff
Spec : EN 55022, Class B
Type : Radiated Polarisation : Vertical

Comments :
SITECOM MM CN-300, ref_1
Karte wird beschrieben



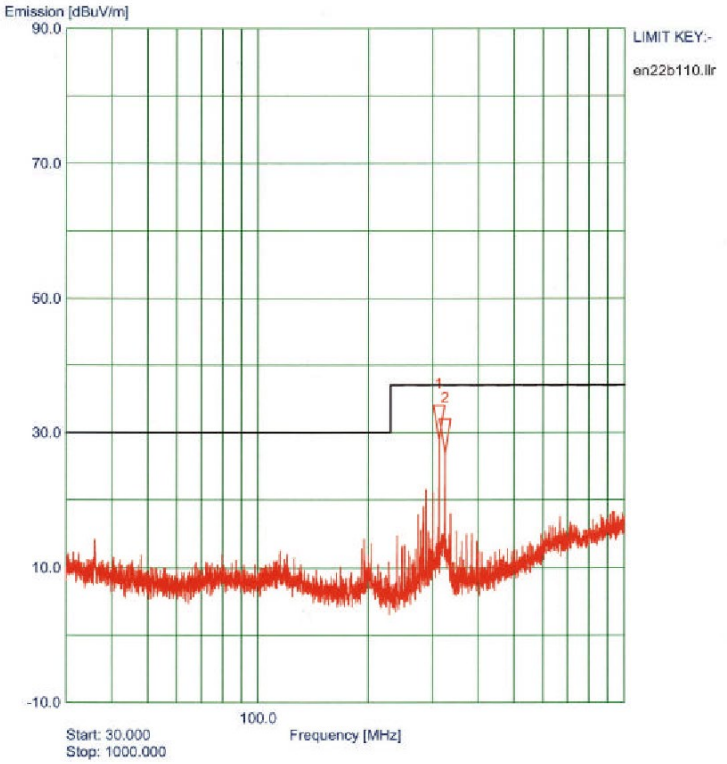
RBW: 120.00 kHz
VBW: 300.00 kHz
Device : CF-Card
Serial #:
Batch : CF-512MS00

23:15:22 16 Jan 2003

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 11

Störfeldstärke - read mode -

Filename : c:\emtest\data\msc\cf_cards\512_21.dat Comments :
Oper : Drotleff SITECOM MM CN-300, ref_1
Spec : EN 55022, Class B Karte wird gelesen
Type : Radiated Polarisation : Vertical



RBW: 120.00 kHz
VBW: 300.00 kHz
Device : CF-Card
Serial #:
Batch : CF-512MS00

23:19:10 16 Jan 2003

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 12

Markers

Test Title:- Störfeldstärke - read mode -
Device Name:- CF-Card
Device Serial No:-
Device Setup No:- CF-512MS00
Operator:- Drotleff
Date/Time:- 16 Jan 2003 23:19:10
Limit Line:- en22b110.li

Marker Data

	Trace		Measured				
Marker	Freq (MHz)	Peak (dBuV/m)	Freq (MHz)	Peak (dBuV/m)	CLP (dBuV/m)	Average (dBuV/m)	Limit (dBuV/m)
1	312.32	29.05	312.05	29.52	26.03	-	37,00
2	324.46	27.01	324.12	23.41	16.52	-	37,00

Nachmessung mit dem Quasipeak-Detektor: geringster Abstand zum Grenzwert = ca. 10 dB

Summary

Control Information

Test Title:- Störfeldstärke - write mode -
Device Serial No:-
Device name:- CF-Card — Device Batch No:- CF-512MS00
Operator:- Drotleff — Date/Time:- 16 Jan 2003 23:15:22
Q.A.:- Code 1 — Report No:-
Approved by:- Dr.
Comments:- SITECOM MM CN-300, ref_1
Karte wird beschrieben

Test & Frequency Ranges

Specification:- EN 55022, Class B
Type:- Radiated — Polarisation:- Vertical

Frequency Ranges:- 1) 30.00 MHz to 42.60 MHz
2) 42.60 MHz to 60.49 MHz
3) 60.49 MHz to 85.90 MHz
4) 85.90 MHz to 121.98 MHz
5) 121.98 MHz to 173.21 MHz
6) 173.21 MHz to 245.95 MHz
7) 245.95 MHz to 349.25 MHz
8) 349.25 MHz to 495.93 MHz
9) 495.93 MHz to 704.23 MHz
10) 704.23 MHz to 1.00 GHz

Parameters

Resolution bandwidth:- 120.00 kHz
Video bandwidth:- 300.00 kHz
Attenuation:- 10dB
Sweep Time:- Auto
No. of sweeps/measurement:- 10

Limit lines

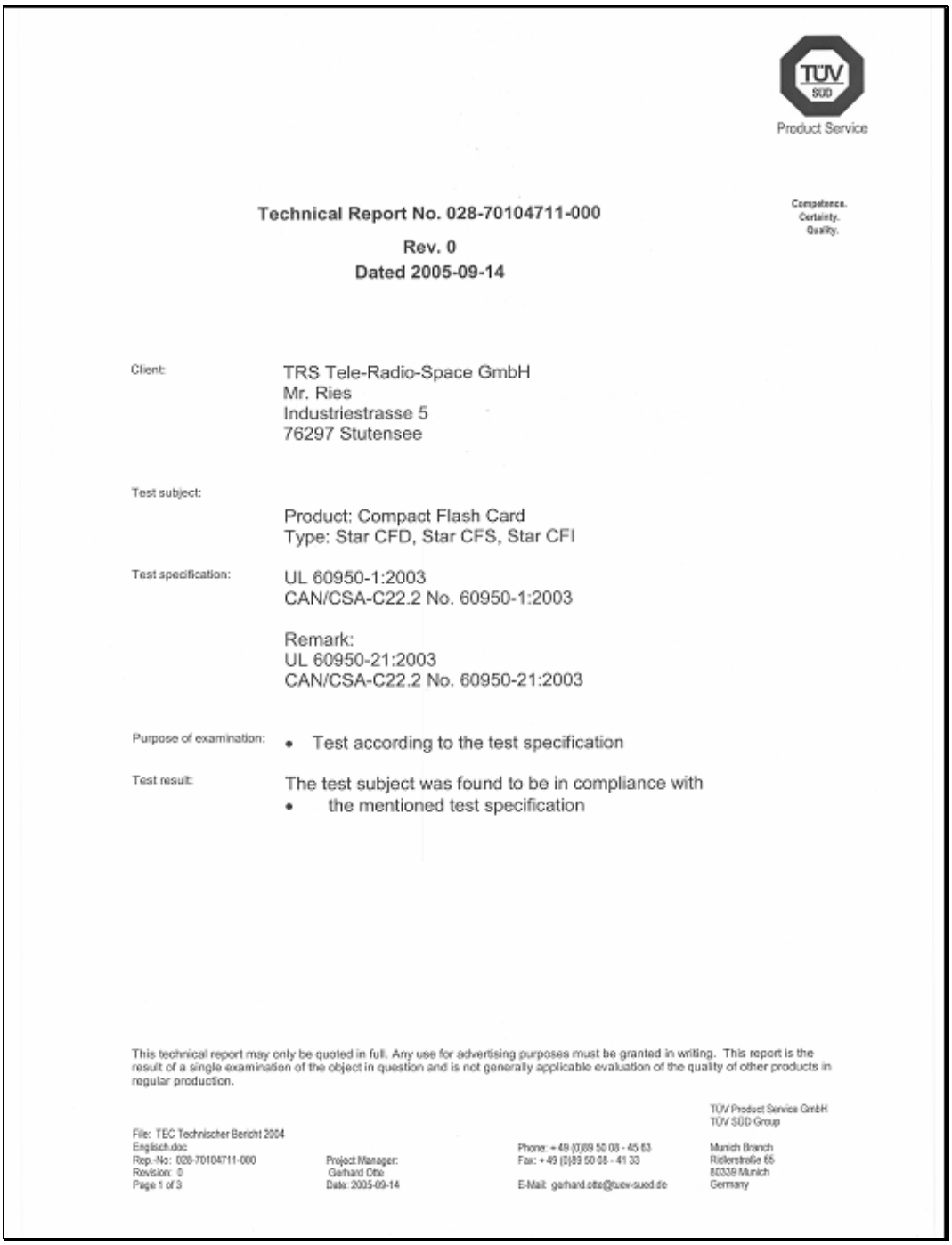
en22b110.llr

Correction factors

hp8447f.amp
h530_e51.xdr

Ing.-Büro DROTLEFF VDI	Report-Nr.: 3041C81	EUT: TRS Star Industrial-Grade	Datum: 24.01.2003	Seite 14

14. NRTL (UL) Technical Report



Product Service

Competence.
Certainty.
Quality.

Technical Report No. 028-70104711-000

Rev. 0

Dated 2005-09-14

Client: TRS Tele-Radio-Space GmbH
Mr. Ries
Industriestrasse 5
76297 Stutensee

Test subject:
Product: Compact Flash Card
Type: Star CFD, Star CFS, Star CFI

Test specification: UL 60950-1:2003
CAN/CSA-C22.2 No. 60950-1:2003

Remark:
UL 60950-21:2003
CAN/CSA-C22.2 No. 60950-21:2003

Purpose of examination:
- Test according to the test specification

Test result: The test subject was found to be in compliance with
- the mentioned test specification

This technical report may only be quoted in full. Any use for advertising purposes must be granted in writing. This report is the result of a single examination of the object in question and is not generally applicable evaluation of the quality of other products in regular production.

File: TEC Technischer Bericht 2004 English.doc
Rep.-No: 028-70104711-000
Revision: 0
Page 1 of 3

Project Manager:
Gerhard Otte
Date: 2005-09-14

Phone: +49 (0)89 50 08 - 45 63
Fax: +49 (0)89 50 08 - 41 33
E-Mail: gerhard.otte@tuev-sued.de

TÜV Product Service GmbH
TÜV SÜD Group
Munich Branch
Ridlerstraße 65
80339 Munich
Germany

Product Service

1 Description of the test subject

1.1 Function

The EUT is intended to be used as data storage device in various applications (e.g. digital cameras, …)

1.2 Technical Data

2 Order

2.1 Date of Purchase Order, Customer's Reference

2005-08-16

2.2 Receipt of Test Sample, Location

2005-08-22

2.3 Date of Testing

2005-08-23 to 2005-09-09

2.4 Location of Testing

TÜV Product Service GmbH
München

Phone: + 49 (0)89 50 08 - 45 63
Fax: + 49 (0)89 50 08 - 41 33

E-Mail: gerhard.otte@tuev-sued.de

TÜV Product Service GmbH
TÜV SÜD Group

Munich Branch
Ridlerstraße 65
80339 Munich
Germany

Product Service

3 Test Results

3.1 Positive Test Results

The tested equipment fulfils the requirements concerning the test standard

4 Remark

The user manual has been examined according to the minimum requirements described in the product standard. The manufacturer is responsible for the accuracy of further particulars as well as of the composition and layout

4.1 Remarks to Factory

The assembly of the product has to comply with the documentation (CDF). Before the implementation of safety relevant modifications to the product into the ongoing production the product must be assessed for acceptance. The results must be implemented to the documentation and if necessary the certificate must be updated.

TÜV Product Service GmbH	TÜV Product Service GmbH
Technical Report checked	Engineer
Ralph Fischer TEC Region South	i.A. Gerhard Otte TEC Region South

File: TEC Technischer Bericht 2004 Englisch.doc
Rep.-No: 028-70104711-000
Revision: 0
Page 3 of 3

Project Manager:
Gerhard Otte
Date: 2005-09-14

Phone: + 49 (0)89 50 08 - 45 63
Fax: + 49 (0)89 50 08 - 41 33
E-Mail: gerhard.otte@tuev-sued.de

TÜV Product Service GmbH
TÜV SÜD Group
Munich Branch
Ridlerstraße 65
80339 Munich
Germany

15. Bibliography

[1] SanDisk Standard Grade – CompactFlash and PC Card –
Product Manual Rev. 1.2
[2] SanDisk Industrial Grade – CompactFlash, PC Card and FlashDrive –
Product Manual Rev. 2.2
[3] CompactFlash Association – CF+ and CompactFlash Specifcation Rev. 2.0

A. Appendix

A.1 CHS (Cylinder-Head-Sector) Information

Table A.1. CHS (Cylinder-Head-Sector) Information

Model No.	Capacity	Cylinder	Head	Sector	Total
STAR CFI-016Mx xxx.yyy.zz	16MB	256	4	32	32 768
STAR CFI-032Mx xxx.yyy.zz	32MB	512	4	32	65 536
STAR CFI-048Mx xxx.yyy.zz	48MB	768	4	32	98 304
STAR CFI-064Mx xxx.yyy.zz	64MB	1 024	4	32	131 072
STAR CFI-096Mx xxx.yyy.zz	96MB	1 536	4	32	196 608
STAR CFI-128Mx xxx.yyy.zz	128MB	1 024	8	32	262 144
STAR CFI-192Mx xxx.yyy.zz	192MB	1 536	8	32	393 216
STAR CFI-256Mx xxx.yyy.zz	256MB	1 024	16	32	524 288
STAR CFI-384Mx xxx.yyy.zz	384MB	1 536	16	32	786 432
STAR CFI-512Mx xxx.yyy.zz	512MB	1 024	16	63	1 032 192
STAR CFI-768Mx xxx.yyy.zz	768MB	1 536	16	63	1 548 288
STAR CFI-001Gx xxx.yyy.zz	1GB	2 048	16	63	2 064 384
STAR CFI-01G5x xxx.yyy.zz	1,5GB	3 072	16	63	3 096 576
STAR CFI-002Gx xxx.yyy.zz	2GB	4 096	16	63	4 128 768
STAR CFI-003Gx xxx.yyy.zz	3GB	6 144	16	63	6 193 152
STAR CFI-004Gx xxx.yyy.zz	4GB	8 192	16	63	8 257 536
STAR CFI-006Gx xxx.yyy.zz	6GB	12 288	16	63	12 386 304
STAR CFI-008Gx xxx.yyy.zz	8GB	16 284	16	63	16 414 272

NOTE: The information is based on the maximum cylinders without spare- and defect cylinders.